HARMONIC REDUCTION TECHNIQUE USING FLYING CAPACITOR BASED Z SOURCE INVERTER FOR A DVR

Deepa S.[1] Rajapandian S.[2]

[1]Research Scholar, Sathyabama University, Chennai
[2]Panimalar Engineering College, Chennai

Abstract

The Dynamic Voltage Restorer (DVR) is a commercially available, popular device to eliminate voltage sags and swells in the distribution lines. Its basic function is to inject the voltage difference (difference between the pre-sag and sag voltage) to the power line and maintains the pre-sag voltage condition in the load side. The efficiency of the DVR depends on the performance of the efficiency control technique involved in switching the inverters. Z-source inverters are recent topological options proposed for buck-boost energy conversion with a number of possible voltage-and current-type circuitries. Common feature noted is their inclusion of an LC impedance network, placed between the dc input source and inverter bridge. This impedance network allows the output end of a voltage-type Z-source inverter to be shorted for voltage boosting without causing a large current flow and the terminal current of a current-type inverter to be interrupted for current boosting without introducing overvoltage oscillations to the system. Therefore, Z-source inverters are, in effect, safer and less complex and can be implemented using only passive elements with no additional active semiconductor needed. This paper presents a selective harmonic elimination using flying capacitor connection in Z-source inverter. Close loop control for a simple system is modeled and simulated using MATLAB software. The simulation results are presented to demonstrate the effectiveness of the proposed DVR system.

Keywords: DVR, Z-source converter, flying capacitor, voltage sag, power quality.

I. INTRODUCTION

The voltage sag/swell is the most common power quality related problem among the industries. Such voltage sag/swell have a major impact on the performance of the microprocessor based loads as well as the sensitive loads. In a power line voltage sags/swells can occur as a result of load switching, motor starting, faults, lightning, non-linear loads, intermittent loads, etc. IEEE 519-1992 and IEEE 1159-1995 describe the Voltage sags/swells as shown in Table 1 and within which controlling equipment should be connected together with the critical loads as corrective measures [1]. IDVR is a commercially available cost effective device, which is capable of addressing the above voltage sag problem effectively.

Table 1. Definitions for voltage sag and swell

Type of disturbance	Voltage	Duration
Voltage Sag	0.1-0.9 pu	0.5-30 cycles
Voltage Swell	1.1-1.8 pu	0.5-30 cycles

II. DYNAMIC VOLTAGE RESTORERS

A DVR is a device that injects a dynamically controlled voltage Vinj (t) in series to the bus voltage by means of a booster transformer as depicted in Figure 1. The amplitudes of the injected phase voltages are controlled such as to eliminate any detrimental effects of a bus fault to the load voltage VL (t). This means that any differential voltage caused by transient disturbances in the AC feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the booster transformer. The DVR works independent of the type of fault or any event that happens in the system, provided that the whole system remains connected to the supply grid, i.e. the line breaker does not trip. For most practical cases, a more economical design can be achieved by only compensating the positive and negative sequence components of the voltage disturbance seen at the input of the DVR. This option is reasonable because for a typical distribution bus configuration, the zero sequence part of a disturbance will not pass through the step down transformers because of infinite impedance for this component. For most of the time the DVR has, virtually, "nothing to do," except monitoring the bus voltage. This means it does not inject any voltage $(V_{inj}(t) = 0)$

independent of the load current. Therefore, it is suggested to particularly focus on the losses of a DVR during normal operation. Two specific features addressing this loss issue have been implemented in its design, which are a transformer design with low impedance, and the semiconductor devices used for switching

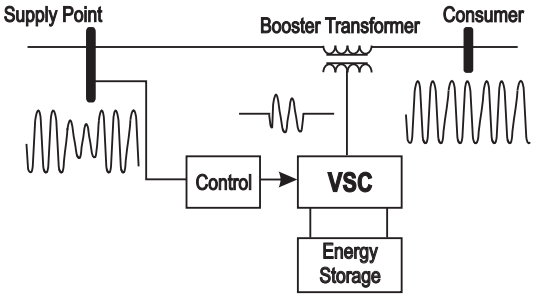

Fig. 1. Schematic diagram of DVR System

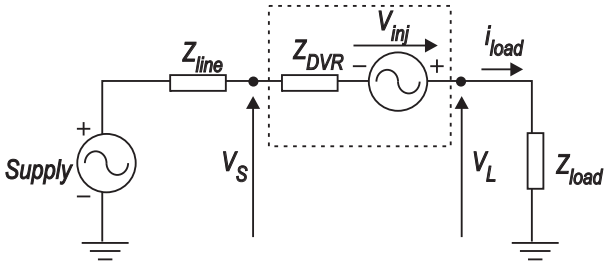

Fig. 2. Equivalent circuit of DVR

Mathematically expressed, the injection satisfies

$$V_L(t) = Vs(t) + V_{inj}(t) \quad ...(1)$$

Where $V_L(t)$ is the load voltage, $V_s(t)$ is the sagged supply voltage and $V_{inj}(t)$ is the voltage injected by the mitigation device as shown in Fig. 2. Under nominal voltage conditions, the load power on each phase is given by

$$S_L = I_L V_L^* = P_L - jQ_L \quad (2)$$

Where I is the load current and PL and QL are the active and reactive power taken by the load respectively during a sag. When the mitigation device is active and restores the voltage back to normal, the following applies to each phase

$$S_L = P_L - j\,Q_L = (P_S - j\,Q_s) + (P_{inj} - jQ_{inj}) \quad (3)$$

where the sag subscript refers to the sagged supply quantities. The inject subscript refers to quantities injected by the mitigation device.

The real and reactive power is given by

$$P_p = |V_p| \sum_{q=1}^{n} |V_q| (G_{pq} Cos\,\delta_{pq} + B_{pq} Sin\,\delta_{pq}) \quad (4)$$

$$Q_p = |V_p| \sum_{q=1}^{n} |V_q| (G_{pq}\,Sin\,\delta_{pq} - B_{pq}\,Cos\,\delta_{pq}) \quad (5)$$

III. Z-SOURCE INVERTER

Z-source inverter has X-shaped impedance network on its DC side, which interfaces the source and inverter H-bridge as shown in Fig. 3. It facilitates both voltage-buck and boost capabilities. The impedance network composed of split inductors and two capacitors. The supply can be DC voltage source of DC current source or AC source. Z-source inverter can be of current or voltage source type.

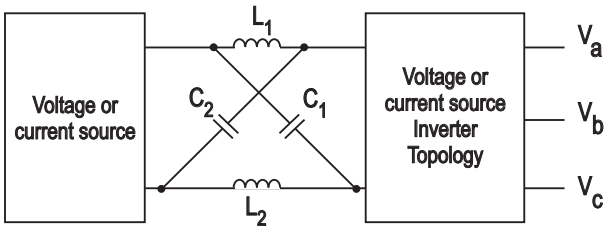

Fig. 3. General Block Diagram of Z-Source Inverter

Z-Source inverter operation is controlled by multiple pulse width modulation. The output of the Z-Source inverter is controlled by using pulse width modulation, generated by comparing a triangular wave signal with an adjustable DC reference and hence the duty cycle of the switching pulse could be varied to synthesize the required conversion. A stream of pulse width modulation is produced to control the switch as shown in the Fig. 4.

In single-phase Z-Source inverter has five switching modes. Two active modes in which the dc source, voltage is applied to load, two zero modes in which the inverter's output terminals are short circuited by S1 and S3 or S2 and S4 switches and a shoot-through mode which occurs as two switches on a single leg are turned on. In a symmetric impedance network, the following equations are valid:

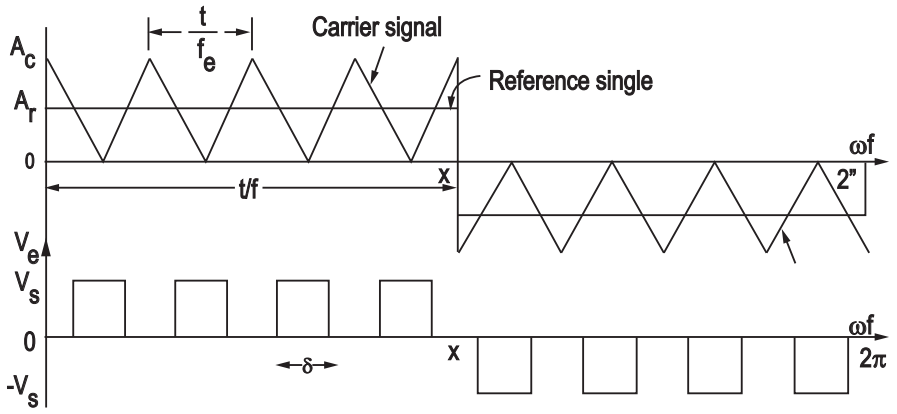

Fig. 4. Multiple Pulse Width Modulation

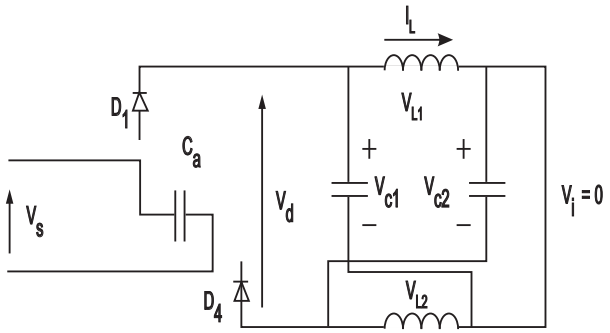

Fig. 5. Shoot through mode

$$C1 = C2 = C \quad (6)$$

$$L1 = L2 = L \quad (7)$$

$$I\,L1 = I\,L2 = I\,L \quad (8)$$

$$V\,C1 = V\,C2 = V\,C \quad (9)$$

The voltage of capacitors in a symmetric impedance network is as follows:

$$V\,i = \beta\,V\,dc \quad (10)$$

$$\beta = 1 / [\,1 - 2\,(T0/T)\,] \quad (11)$$

Where, T0 and T show the shoot-through mode application period and switching period, respectively. Also, the following relation is valid in symmetric impedance networks:

$$Vi = 2VC - Vdc \quad (12)$$

It should be noted that the relations mentioned above are extracted by averaging the ZSI operational modes. The shunt full bridge rectifier with the input capacitor Ca which feeds the impedance network is shown in Fig. 6. During the commutation between diodes, it is possible to face with surge voltage due to line inductance and shoot-through mode operation. The input capacitor is used to suppress this surge voltage. Diodes D1 and D4 are turned on if the input voltage of rectifier is positive. Diodes D3 and D2 are turned on if the input voltage of rectifier is not positive.

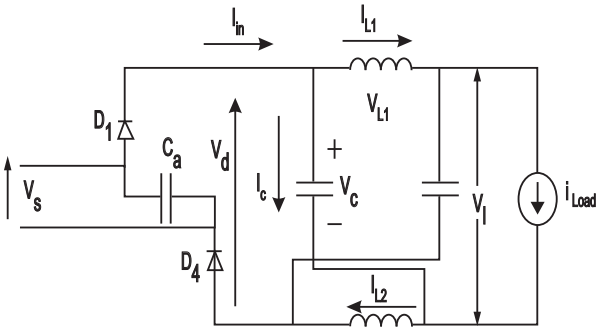

Fig. 6. Active modes

The equivalent circuits of rectifier fed ZSI in shoot-through and active modes are presented in Figs. 5 and 6 respectively. The following is obtained according to that equivalent circuit:

$$Vd = VL1 + VC2 \quad (8)$$

$$VL1 = VC1 \quad (9)$$

Where Vd is the impedance network input voltage.

IV. VOLTAGE SAG COMPENSATION IN DVR SYSTEM

The performance of the designed DVR as shown in Figure 7 and Figure 8 is evaluated using Matlab/Simulink. The proposed method was tested for voltages sag in the low voltage distribution system

In case of voltage sag, the source voltage has decreased about 20-25% of its nominal value. It shows the grid voltage which has dropped to 25% at t = 0.3 sec and the sag lasts 0.7 sec and then voltage will restore back to its normal value. The function of the DVR will injects the missing voltage in order to regulate the load voltage from any disturbance due to immediate distort of source voltage.

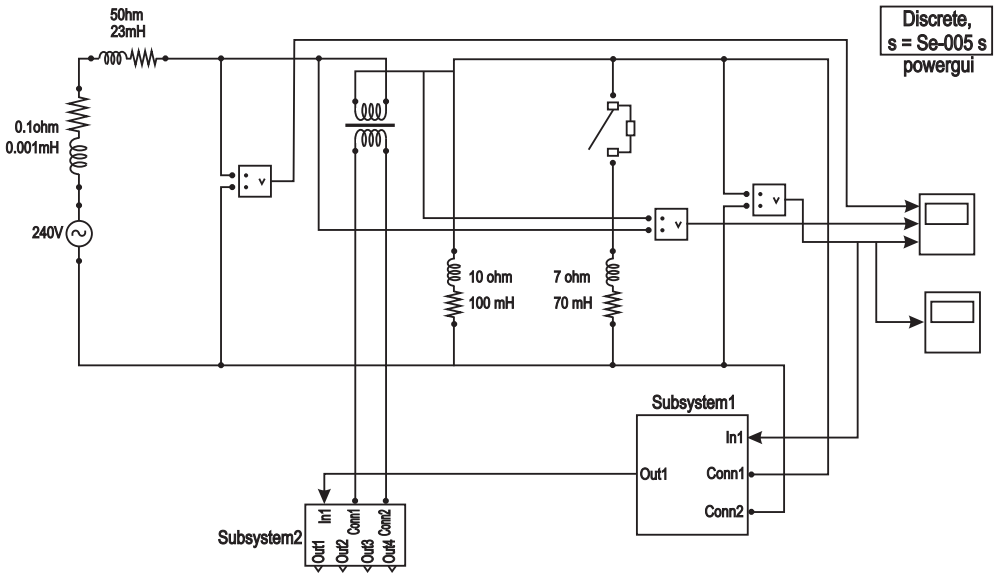

Fig 7. Voltage Sag Compensation in a DVR System

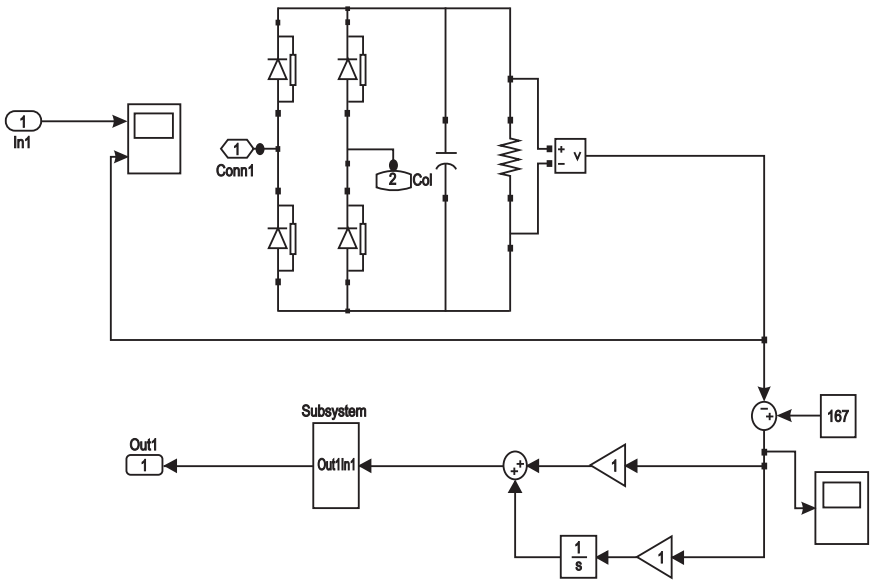

Fig. 8. Subsystem 1 of Closed Loop Control of Voltage Sag Compensation in a DVR System

Fig. 8. shows the subsystem 1 of the closed loop DVR system. It contains the PI controller. The AC output voltage is rectified to DC supply and then a reference voltage is given for the error. This error is sent to the PI controller. The saturator value is given as pulses for controlling the Z-Source inverter. In the Fig 9. subsystem 2 contains the Z-Source inverter which is being controlled by the PI controller. The Z-Source starts conducting when it obtains the pulse from the saturator. Fig. 10. shows the output waveform

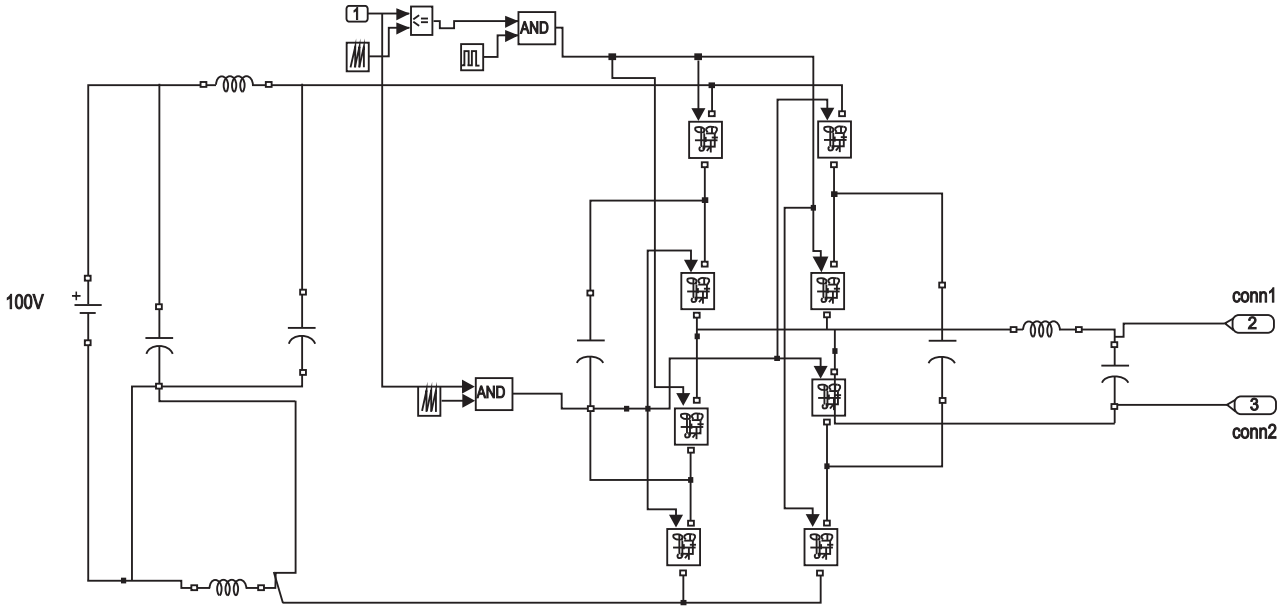

Fig. 9. Sub system 2 of Closed Loop Control of Voltage Sag Compensation in a DVR System

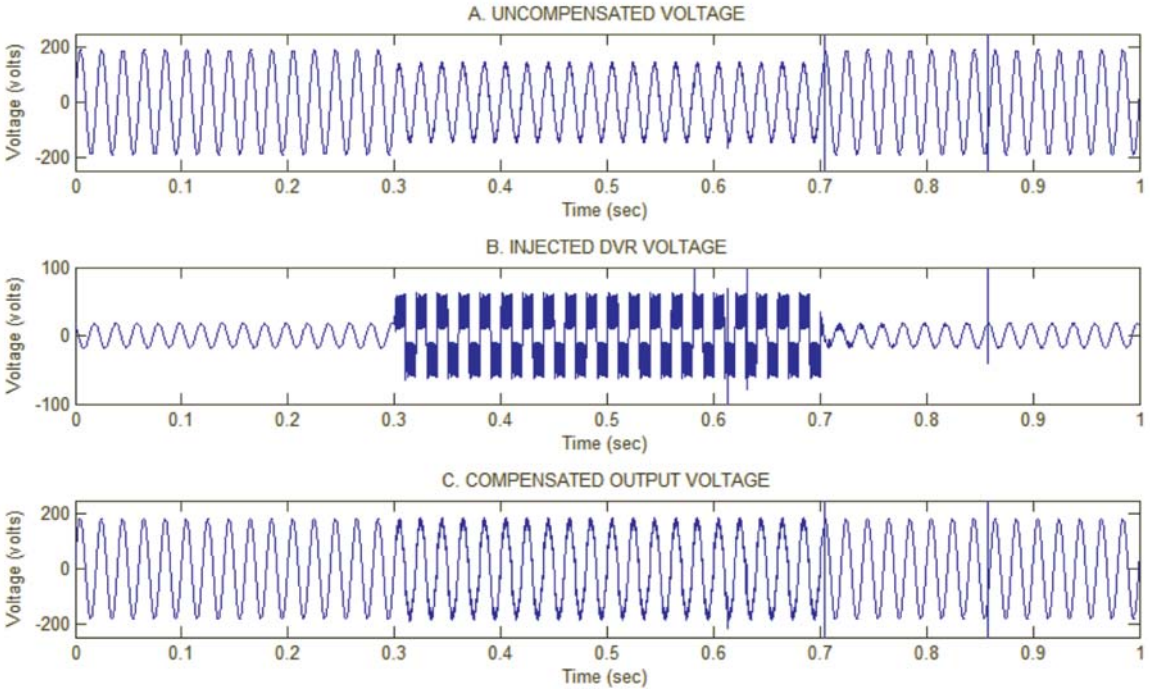

Fig. 10. Simulation results of Closed Loop Control DVR with 30% swell (a) Uncompensated Voltage, (b) Injected DVR Voltage, (c) Compensated Voltage

of closed loop control of voltage sag compensation. Fig. 10.(a) shows the uncompensated AC voltage with 25% sag. Fig. 10.(b) shows the injected DVR voltage. Fig. 10.(c) gives the compensated output voltage.

In Fig. 11. FFT analysis is performed for the compensated output voltage. Here the Total Harmonic distortion (THD) for firing angle a = 60 is 0.32%. In flying capacitor based Z-source inverter selective harmonics can be eliminated. For example if we trigger the z-source inverter at angle of 60 we can eliminate third order harmonics. Table 2. shows THD value for different firing angle. The load voltage is maintained at the same value throughout the simulation. Thus voltage sag compensation using closed loop control is simulated.

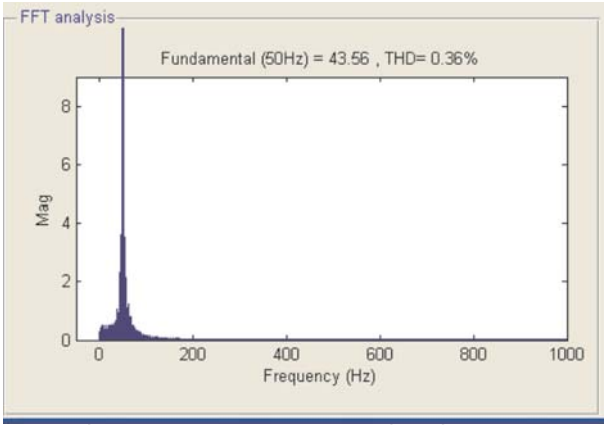

Table 2. Voltage harmonics for different values of firing angle (a)

α	THD		Harmonic eliminated order
	Conventional method	Proposed method	
Degree	(%)	(%)	n
25.5	1.52	0.13	7^{th}
36	1.48	0.25	5^{th}
60	1.89	0.36	3^{rd}

V. CONCLUSION

Hence the simulink model for 20% of voltage sag compensation is modeled and simulated. The respective THD values are obtained is shown.Voltage Sag Compensation Conventional Z source inverter = 1.55%. Modified Z source inverter = 0.36% The voltage compensation for both sag and swell can be implemented in a three phase DVR system for various types of modulations.

REFERENCES

[1] A. Ghosh and G. Ledwich, "Power Quality enhancement Using Custom Power Devices", Kluwer Academic Publishers, (2002).

[2] S. Santoso, "Electrical Power System quality," Mcgraw-Hill, 2002.

[3] N.G. Hingorani, "Introducing Custom Power, in IEEE Spectrum", 32, pp. 4l-48, (1995).

[4] P.T. Nguyen and T.K. Saha, "DVR against balanced and unbalanced Voltage sags: Modeling and simulation," IEEE-School of Information Technology and Electrical Engineering, University of Queesland, Australia, 2004.

[5] Yop Chung, Dong-Jun Won; Sang-Young Park; Seung-Il Moon and Jong-Keun Park; "The DC lin energy control method in dynamic voltage restorer system", International journal on Electric power and energy system, Volume 25, Issue 7, September 2003, Pages 525-531.

[6] Paisan Boonchiam and Nadarajah Mithulananthan, "Understanding of Dynamic Voltage Restorers Through MATLAB Simulation" Thammasat Int. J. Sc. Tech., Vol.11, No.3, July-September 2006.

[7] B. Justus Rabi and R. Arumugam, "Harmonics Study and Comparison of Z-Source Inverter with Traditional Inverters", American Journal of Applied Sciences 2 (10): 1418-1426, (2005).

[8] Shen, M.; Joseph, A.; Wang, J.; Peng, F.Z.; Adams, D.J. "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles", IEEE Power Electronics in Transportation: 125-132 (2004).

[9] F.Z. Peng, "Z-Source Inverter," in Proc. IEEE IAS' pp.775-781.02 (2002).

S.Deepa has obtained her B.E degree from Periyar University in 2003. She has obtained her PG degree from Annamalai University in 2005. Presently she is doing her research at Sathyabama University. Her research interest is in the area of Power quality.

Dr. S. Rajapandian has obtained his B.E degree from Madras University in 1966. He obtained his M.E degree and PhD from IISc, Bangalore in 1969 and 1974. Presently he is Principal of Panimalar Engineering College, Chennai, India. He is also Senior Professor in Sathyabama University and visiting Professor of Anna University. His research interest is in areas of High voltage Engineering and capacitors.