COMPARISON OF PERFORMANCE OF SINGLE IMPEDANCE NETWORK BASED NEUTRAL POINT CLAMPED THREE LEVEL AND SEVEN LEVEL THREE PHASE INVERTER WITH REDUCED CLAMPING DIODES

Kuppuswamy C.L.[1], Raghavendiran T.A.[2]

[1]Research Scholar, Sathyabama University, Chennai
[2]Anand Institute of Higher Technology, Chennai
Email: [1]clkuppuswamy@gmail.com, [2]aiht_anand@yahoo.co.in[2]

ABSTRACT

This paper presents a comparative analysis of performance of three level and seven level Z-source Neutral Point Clamped (NPC) multilevel inverter. A single impedance network is used irrespective number of levels. The Z-source will help in boosting the DC voltage of renewable energy such as fuel cells and photovoltaic cells. Z-source multilevel Inverter will act as a booster inverter and also due to the presence of source impedance network, it provides ride through shoot through faults and by suitable impedance matching the common mode signals are also eliminated. A seven level inverter with reduced number of devices is presented. Since the number of devices are reduced compared to the conventional topologies, the proposed Z-source inverters are compact, energy efficient and cost effective. The simulation and experimental results are presented to demonstrate the benefits of these topologies.

Key words: Three level inverter, Seven level inverter, Renewable Energy Sources, NPC inverter, Z-source Multilevel inverter, Single Impedance network.

I INTRODUCTION

The transfer of power from the Renewable energy sources to grid or loads requires DC-AC converters. The Z-source NPC is a kind of single stage multilevel inverter which has the ability of voltage boost [1], But the boost capability is relatively low when they are subject to the renewable sources. The Z-source converter employs an impedance circuit which connects the power source to the converter circuit thus providing unique features that cannot be obtained in the conventional Voltage Source Inverter (VSI) and Current Source Inverter (CSI) [4]; where a capacitor and inductor are used respectively [9]. The Z-source inverter overcomes limitations of the traditional VSI and CSI. The conventional voltage source inverter (VSI) can only produce an output voltage that is lower than the supply voltage of the battery. The maximum output voltage obtainable is limited by the dc bus voltage. For battery supplied electric vehicles, the dc-dc boosted inverter has the useful feature to either buck or boost the batteries voltage to a desired output voltage. To obtain high voltage from hybrid sources, dedicated impedance networks are connected for each source [2]. A Hybrid Pulse Width Modulation (PWM) technique combines the space-vector PWM with the ease of implementation of a triangular-comparison PWM. Such strategy reduces the effort of the algorithm calculation [3]. These PWM controlling techniques can be easily applied to Cascaded MLI but cascaded MLI requires separated DC sources [3, 5]. To overcome this drawback NPC inverters are better choice [10, 13]. But applying space vector modulation for these inverters is very complex [7-9]. A Z-source NPC inverters offers less distorted high output voltage [12, 15, 16] which can meet high power demand [11]. A seven level NPC with single impedance network and reduced clamping diodes is proposed in this paper which employs multiple carrier signal modulation technique which can be used for regenerative applications because the re-generated energy can be stored in capacitor and inductor of impedance network [17]. Peng et al. [12] have proposed an ac–dc–ac converter formed by cascading a two-level Z-source dc–ac inverter to a front-end diode rectifier in AC-DC-AC converters. As first described in [6], the Z-source inverter allows the system output voltage to be stepped down or up as desired by inserting a unique X-shaped LC impedance network, comprising two inductors and two capacitors, between the rectifier and inverter circuitries. This paper presents the performance of single impedance network based three and seven level NPC inverter which can be used for AC drives, as active filters or by employing suitable control devices they can also be used as FACTS devices.

II Z-SOURCE MULTILEVEL NPC INVERTER

The block diagram of proposed topologies is shown in Fig. 1. The input DC is given to NPC (three/seven) multilevel inverter. The output of multilevel inverter may be injected to micro grid or it may be used to drive the loads.

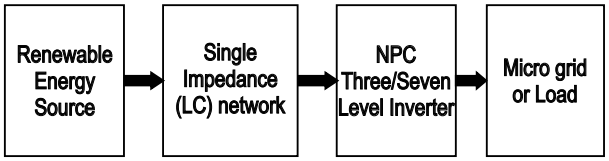

Fig. 1. Block diagram of proposed Topology

III SIMULATION RESULTS FOR Z-SOURCE THREE LEVEL NPC INVERTER

The simulation is carried out using MATLAB/Simulink. The simulation circuit is shown in Fig. 2. Input is 48V DC which is shown in Fig. 3.

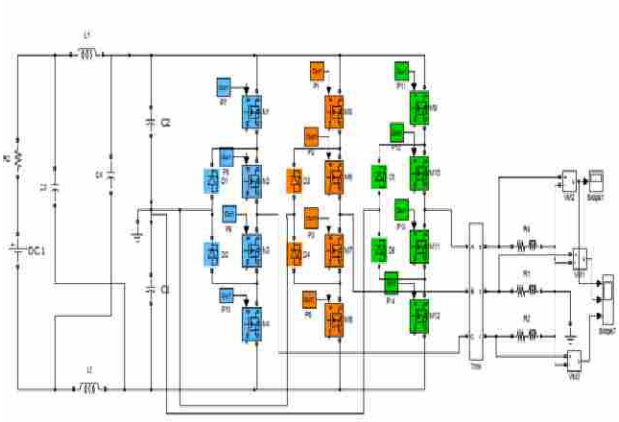

Fig. 2. Simulation circuit diagram of prosed Z-source Three Level NPC inverter

The gate pulses for MOSFET's in first leg M1 - M4 are shown in Fig. 4. The phase output voltages in Leg 1 are shown in Fig. 5. The proposed inverter Phase volatges in all three legs are shown in Fig. 6. The line voltages of three phase three level Z-source inverter are shown in Fig. 7. Three pahse currents are shown in Fig. 8. The FFT analysis is done to find the Total Harmonic Distortion (THD) and the FFT results are shown in Fig. 9.

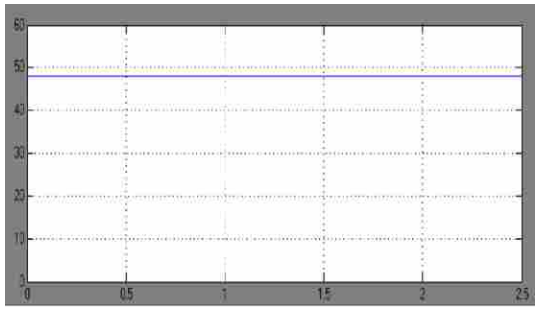

Fig. 3. DC Input Voltage T(ms)

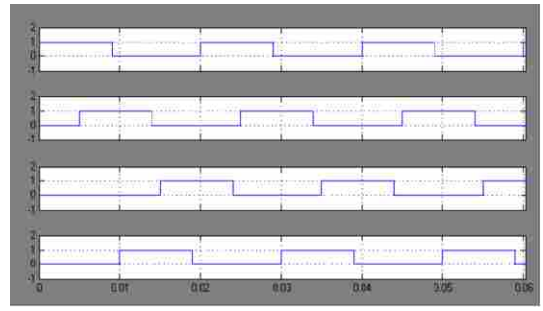

Fig. 4. MOSFET Gate Pulses (I- Phase)

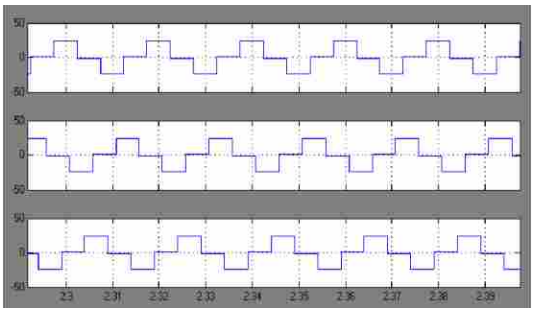

Fig. 5. Phase Voltages in Leg 1 (I-Phase)

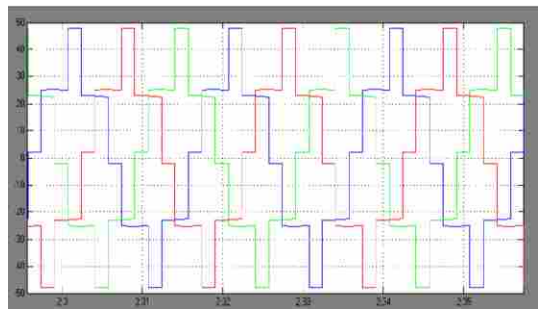

Fig. 6. Per Phase Voltage in Three Legs

As observed from Fig. 6, three levels 48 V, 24 V and Zero voltages are obtained. From this it is concluded that a single impedance network is sufficient to obtain the required levels. In conventional topologies the maximum voltage will be less than the input DC supply voltage since there will be voltage drop across the solid state devices.

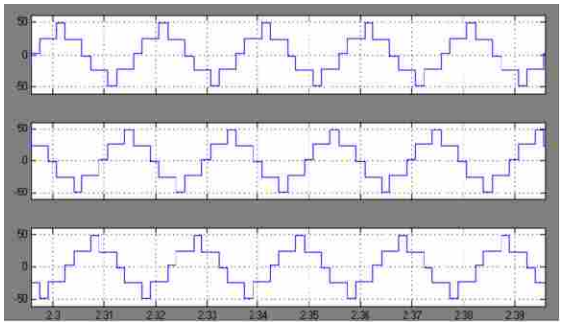

Fig. 7. Line Voltages of proposed circuit

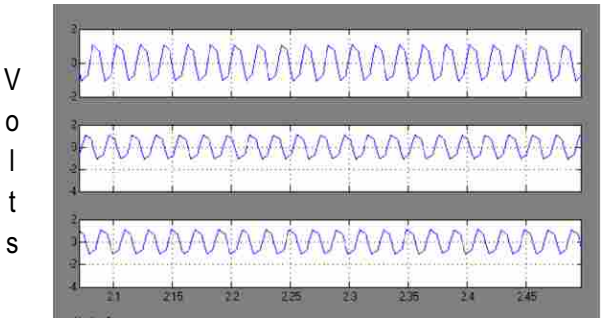

Fig. 8. Three Phase Output Currents

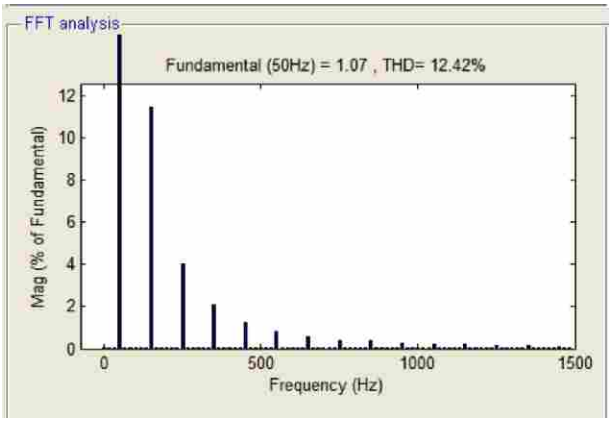

Fig. 9. FFT Analysis Results.

The THD of the Z-Source three level inverter is 12.42%.

IV EXPERIMENTAL RESULTS FOR Z-SOURCE THREE LEVEL NPC INVERTER

The experimental set up is shown in Fig. 10. To illustrate the merit of the proposed topology, the Inductances are designed and capacitances are selected to boost a voltage of 26 V to 70 V. The input voltage is shown in Fig. 11. The driver output is shown in Fig. 12. The complementary switching pulses for upper and lower switches are shown in Fig. 13. The inverter output voltage is shown in Fig. 14.

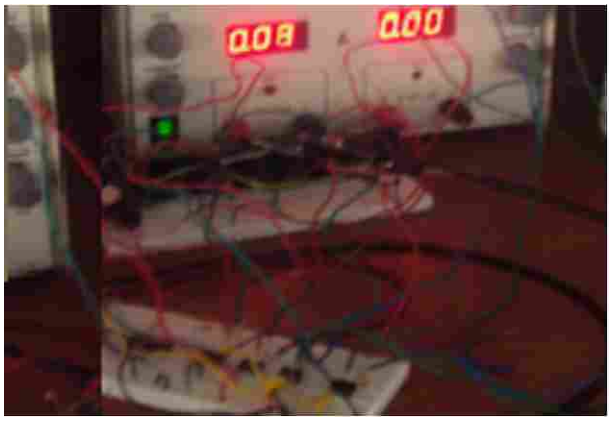

Fig. 10. Experimental Set up

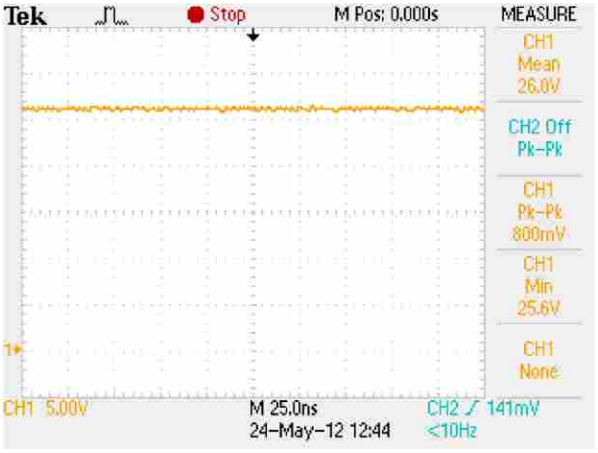

Fig. 11. Input voltage

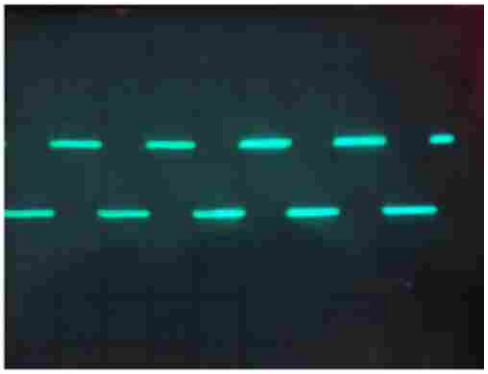

Fig. 12. Output of Driver circuit

Fig. 13. MOSFET Switching pulses

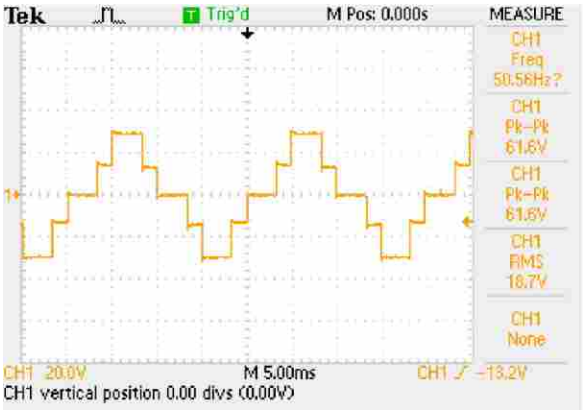

Fig. 14. Inverter Output voltage

V SEVEN LEVEL NEUTRAL POINT CLAMPED Z-SOURCE INVERTER

The basic circuit for single phase seven level neutral point (diode) clamped Z-source inverter is shown in Fig. 15. It consists of 12 main switches, 19 clamping doides. In conventional topologies (m - 1) (m - 2) i.e. 42 clamping diodes per phase are used for balancing the voltage. Therefore all together for three phase inverter clapming diodes are reduced by large number. Each capacitor has the same voltage Em, which is given by

$$E_m = \frac{V_{dc}}{m-1}$$

The output voltage during the positive half-cycle can be found from the equation

$$V_{ao} = \Sigma_{n=1}^{m} E_n SF_n$$

Where SFn is the switching or control function of nth node and it takes a value of 0 or 1. To ontain seven levels, the required switcing scheme is given in Table 1.

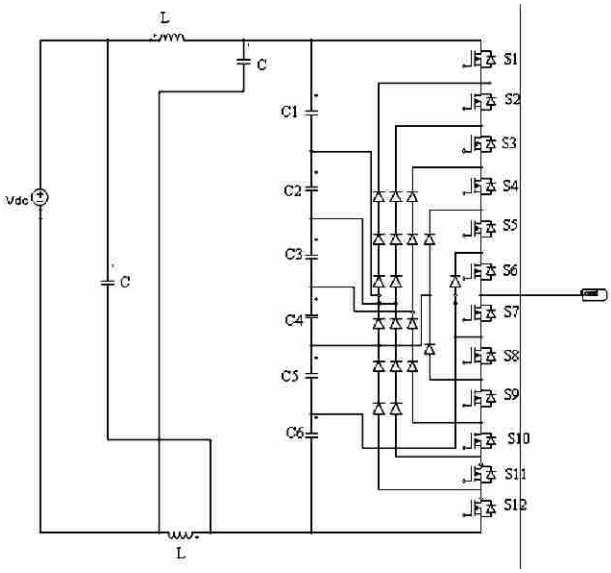

Fig. 15. Single phase seven level neutral point clamped inverter with reduced number of clamping diodes

Table 1 MOSFET switching Table

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
+3 Vdc	1	0	0	1	1	0	0	1	1	0	0	1
+2 Vdc	1	0	0	1	1	0	0	1	1	0	1	0
+1 Vdc	1	0	0	1	0	1	0	1	1	0	1	0
0	1	0	1	0	0	1	0	1	1	0	1	0
−1 Vdc	0	1	1	0	0	1	1	0	1	0	0	1
−2 Vdc	0	1	1	0	0	1	1	0	0	1	0	1
−3 Vdc	0	1	1	0	0	1	1	0	0	1	1	0

VI SIMULATION RESULTS FOR Z-SOURCE THREE LEVEL NPC INVERTER

Simulation circuit of three phase z-source seven level NPC is shown in Fig. 16. Input is 48 V DC shown in Fig. 17. Switching pulses for upper and lower switches are shown in Fig. 18 and Fig. 19 respectively. Seven level inverter output voltage of first phase is shown in Fig. 20 and three phase output currents are shown Fig. 21. The line voltages are shown in Fig. 22. The FFT analysis result is shown in Fig. 23.

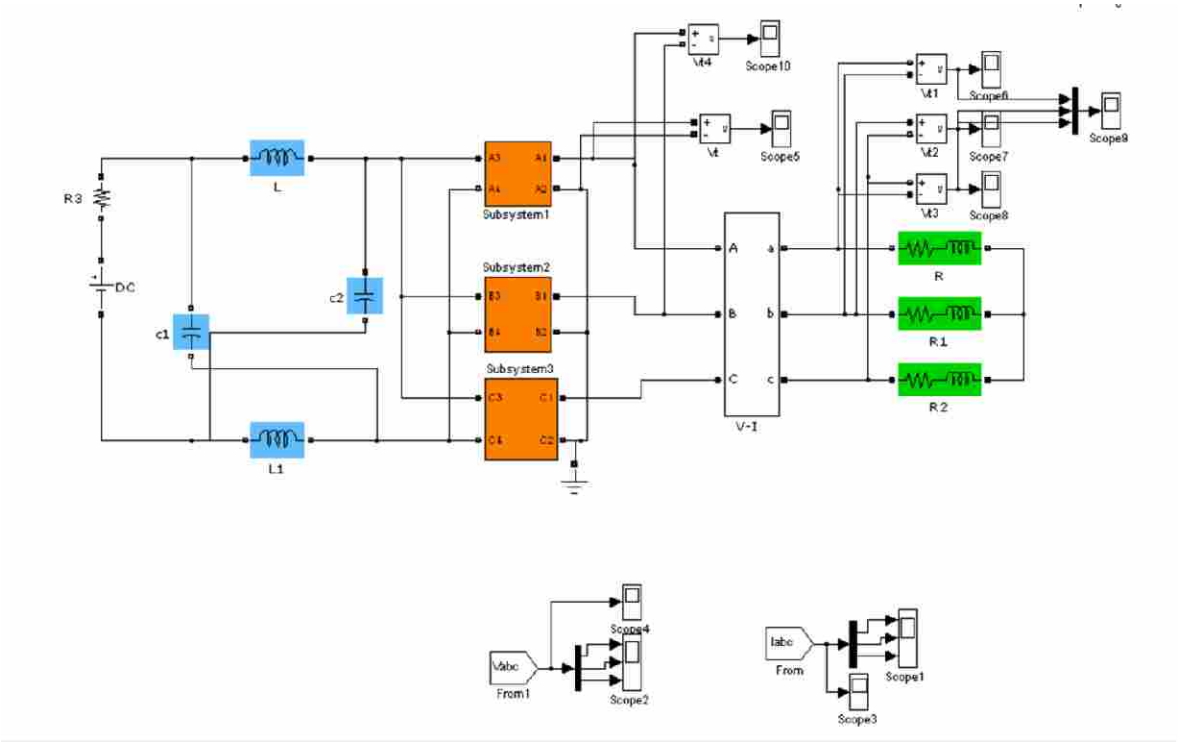

Fig. 16 Simulation circuit diagram of prosed Z-source Seven Level NPC inverter

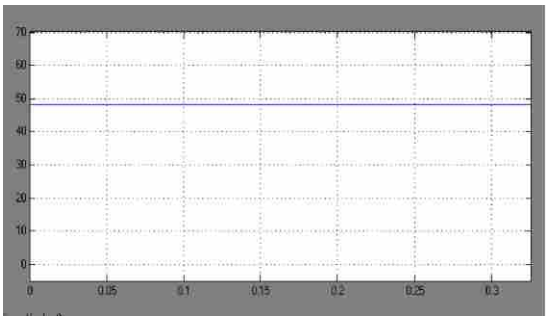

Fig. 17. Input Voltage T (s)

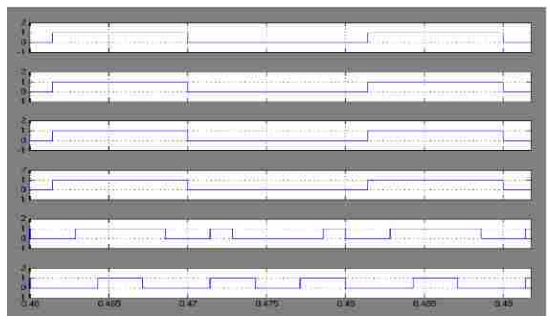

Fig. 18. Switching pulses for Upper switches T (s)

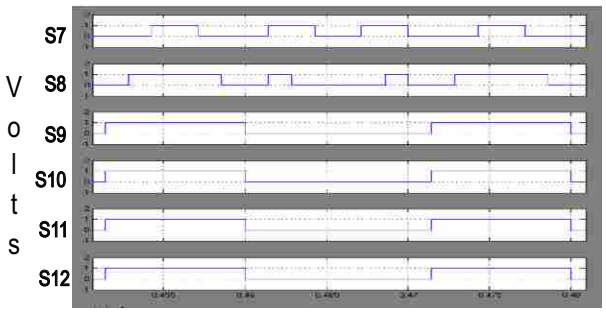

Fig. 19. Switching pulses for Lower switches T (s)

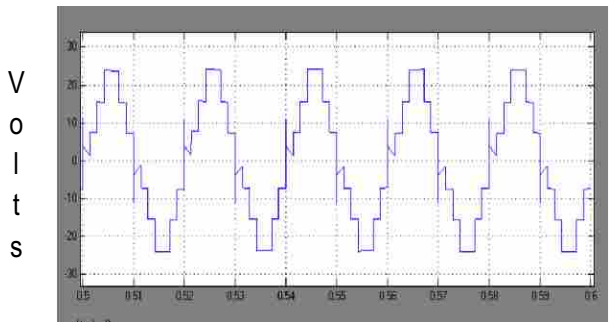

Fig. 20. Phase voltage of first phase T (s)

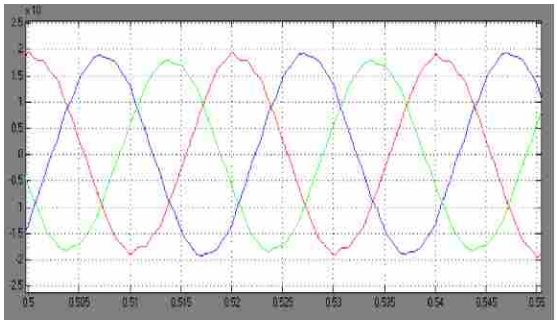

Fig. 21. Three Phase Currents T (s)

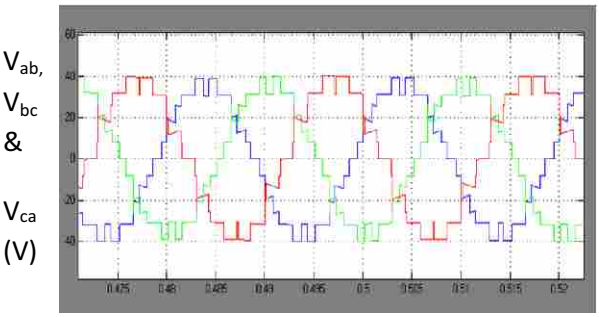

Fig. 22. Line Voltages T (s)

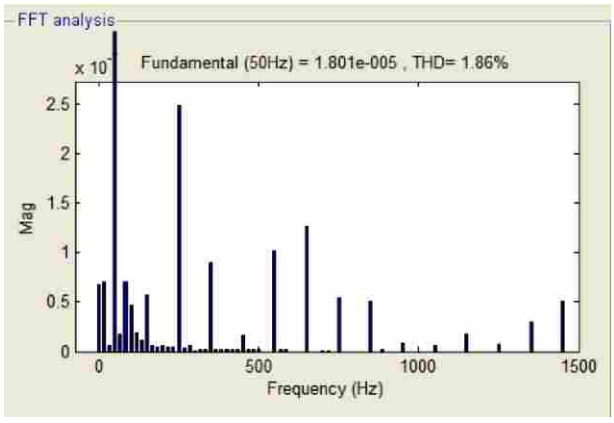

Fig. 23. FFT Analysis Results T (s)

The THD of Z-source modified seven level NPC inverter is 1.86%

VII EXPERIMENTAL RESULTS

The result of the experiment is shown in Figs 24 and 25

Fig. 24 Experimental set up

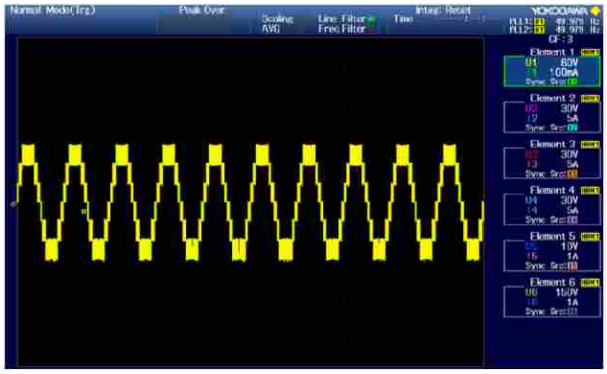

Fig. 25 Inverter Output Voltage

VIII CONCLUSION

So far Z-source network was used for cascaded multilevel inverter and for NPC inverter fed from hybrid sources. Multiple Z-source networks were used for both configurations. A novel single Z-source three and seven level NPC inverter with less number of clamping doides is proposed. The MOSFET internal capacitance and body doides are used for active clamping. This eliminates the need for snubber circuit and hence the snubber losses are reduced. From the simulation results, it is observed that there is slight distortion in the output voltages and currents which can be further reduced by adapting suitable controlling technique. The comparative results for single Z-source, three and seven level NPC inverter are given in Table 2. Since single impedance network is used and clamping diodes are less in number, overall cost and size of the

proposed topologies is reduced. Further the simulation results can be experimentally verified.

Table 2 Comparison Results

Description	Z-source Three Level NPC Inverter	Z-source Seven Level NPC Inverter
Number of Diodes (For 3 φ)	06	57
Number of Switches (for 3 φ)	12	36
Input Voltage	26 V	26 V
Output Voltage	61.6 V	60 V
THD	12.42%	1.86%

REFERENCES

[1] Ying Cheng, Chang Qian, Mariesa L. Crow, Steve Pekarek, "A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM With Energy Storage" Industrial Electronics, IEEE Transactions on power electronics, Volume 53, Issue 5, Oct. 2006 Page(s): 1512 - 1521.

[2] Ding Li, Feng Gao, Poh Chiang Loh, Miao Zhu and Frede Blaabjerg, "Cascaded Impedance Networks for NPC Inverter", Proceedings of IPEC conference, 2010, Vol.4, No.10, pp.1176-1180.

[3] J.H.G. Muniz, E.R.C. da Silva, E.C. dos Santos Jr., "A Hybrid PWM Strategy for Z-Source Neutral-Point-Clamped Inverter", IEEE transactions on industrial electronics, Vol.2, No.11, 2011, pp.450-456.

[4] Said Barkati, Lotfi Baghli, EL Majid Berkouk, Mohmed-Seghir Boucherit, "Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms", Elsevier Electric Power System Research, Vol.78, pp.1736-1746, 2008.

[5] Ebrahim Babaei, Seyed Hossein Hosseini, "New Cascaded Multilevel Inverter Topology with Minimum Number of Switches", Elsevier Energy Conversion and Management, Vol.50, pp.2761-2767, 2009.

[6] Jose Rodriguez, Steffen Bernet, Peter K. Steimer, and Ignacio E. Lizama "A Survey on Neutral-Point-Clamped Inverters" IEEE transactions on industrial electronics, Vol.57, No.7, july 2010, pp.2219-2010.

[7] D. Floricau, E. Floricau and G. Gateau, "Three-level active NPC converter: PWM strategies and loss distribution," in Proc. IEEE IECON, Nov. 2008, pp.3333-3338.

[8] J.I. Leon, S. Vazquez, R. Portillo, L.G. Franquelo, J.M. Carrasco, P.W. Wheeler and A.J. Watson, "Three-dimensional feed forward space vector modulation applied to multilevel diode-clamped converters," IEEE Trans. Ind. Electron., Vol.56, No.1, pp.101-109, Jan. 2009.

[9] M. von Zimmer, M. Lechler, B. Piepenbreier, "Z-Source Drive Inverter using modified SVPWM for low Output Voltage and regenerating Operation", 13th European Conference on Power Electronics and Applications paper 0634, 2009.

[10] J. Rodriguez, L.G. Franquelo, S. Kouro, J.I. Leon, R.C. Portillo, M.A.M. Prats and M.A. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE, Vol.97, No.11, pp.1786-1817, Nov. 2009.

[11] S.M. Dehghan E. Seifi M. Mohamadian R. Gharehkhani "Grid Connected DG Systems Based on Z-Source NPC Inverters", IEEE conference on Power Electronics, Drive systems and technologies, 2011, pp.104-111.

[12] F.Z. Peng, M. Shen and K. Holland, "Application of Z-Source Inverter for Traction Drive of Fuel Cell Battery Hybrid Electric Vehicles," IEEE Transactions on Power Electronics, Vol.22, No.3, pp.1054-1061, 2007.

[13] Panagis, P., F. Stergiopoulos, P. Marabes, and S. Manias, 2008. "Comparison of State of the Art Multilevel Inverters", IEEE Power Electronics Specialists Conference 2008, 15-19 June 2008, pp.4296-4301.

[14] Saravanan V., R. Ramanujam and M. Arumugam "A New Class of Improved & Embedded Z Source Inverters", European Journal of Scientific Research ISSN 1450-216X Vol.69 No.2 (2012), pp.197-208.

[15] C.L. Kuppuswamy, T.A. Raghavendiran, "An Efficient Active Clamped Three Phase Neutral Point Clamped Seven level Inverter with Reduced Switching Stresses and Less Total Harmonic Distortion" in European Journal of Scientific Research, ISSN 1450-216X Vol.78 No.2 (2012), pp.239-247

[16] C.L. Kuppuswamy, T.A. Raghavendiran, "An Efficient Single Impedance Network Three Level Z-Source Neutral Point Clamped Inverter" in IJCSI International Journal of Computer Science Issues, Vol.9, Issue 4, No.2, July 2012, ISSN 1694-0814 Vol.9 Issue 4 (2012), pp.399-403.

[17] C.L. Kuppuswamy, T.A. Raghavendiran, "A Novel Single Impedance Network Based Neutral Point Clamped Seven Level Three Phase Inverter with Reduced Clamping Diodes for Regenerative Applications" in Indian Journal of Computer Science

and Engineering (IJCSE), ISSN:0976-5166, Vol.3 No.4 Aug-Sep 2012, pp.532-538.

C.L. Kuppuswamy received his M.E degree in Power Electronics and Industrial Drives from Sathyabama University, Chennai, India in 2010. He is currently pursuing PhD in Electrical Engineering at Sathyabama University, Chennai. His research interests are Efficient Converter for high power applications and Multilevel Inverters.

Dr. T.A. Raghavendiran received his PhD degree in Anna University, Chennai. He is having 32 years rich experience in Academic and Industries. He has presented number of papers in the Journals and International publications. He is presently working as Principal in Anand Institute of Higher Technology, Chennai India. His area of interest includes Power Quality, Drives & Energy Systems.