Design and Implementation of Low Power CMOS PLL Frequency Synthesizers

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Abstract

One of the important most generally used frequency synthesizer is based on the Phase Locked Loop, which is a building block of the transceiver. Carrier generation can be performed by the frequency synthesizer and it is used for up/down conversion operations. Conversion operation is also a critical block in transceiver, due to the operations carry out at high frequency, takes a huge portion of the entire power consumption on the transceiver side. The main objective of this paper is to design a critical block for frequency synthesizer with minimal power consumptions. Here the proposed design includes XOR PD, Low power LPF, Low power VCO and Parabolic correction blocks which give low power utilization with high accuracy and a reduction in the complexity of the system in terms of hardware and memory usage.

We can achieve better performance from this architecture in terms of low power. The proposed PLL synthesizer is simulated in MATLAB software and the results are shown that the power utilization is very less than the existing approaches.

Keywords: Frequency Synthesizer, Phase Lock Loop, CMOS, Transceiver in Wireless Networks

I. INTRODUCTION

At the recent trend wireless communications is gaining popularity in this electronic world. In a fully integrated system to meet the stringent and the most conflicting requirements, the frequency synthesizer plays a major challenge. The frequency synthesizer is able to generate frequencies of high accuracy and precision. This device incorporates a switched capacitor which will work automatically in order to expand the overall frequency [1]. This is kept at 20MHz/V to improve noise performance. The synthesizer tries in achieving a phase noise. It was recorded as 102dBc/Hz at the offset frequency range of 10KHz. CMOS chips, which are being used in the integrated design requires less power using only one transistor. In the design large output voltage is taken into account to improve oscillator phase noise. It results in inefficient usage of power due to the poor factor of CMOS.

High performance was expected in every design. It includes all the layout techniques and also passive components. The system is designed with careful planning of frequency to meet the requirements. It also provides high performance With the advancement of CMOS technology, in less power technologies it is expected to achieve better performance. It is migrated to 0.35 or even to 0.18-m. FS paves the way to a frequency hopped CMOS. FS is the most important and critical block embedded in wireless transceiver. Whereas the FS is limited by VCO (voltage controlled oscillator) and high frequency divider. It also plays a main role in carrier generation for all the operations such as down or up conversions. The limitation is because of its high frequency operation and consumption of a large part of the power in transceiver.

Nowadays the demand for wireless networks is at a peak rate. This can even support data in the rate of 20 MB/s. This rate is provisioned at lower cost and minimum power consumption. In the recent days the frequency band is intended to provide 300 MHz of spectrum at 5GHz at a wide band level. The synthesizer phase noise requires a dynamic range and bandwidths of wider channel. FS consumes about 20% – 30% of the total power. A typical model comprises of high to low frequency blocks of higher cost. This will be overcome by the application of CMOS technology. Whereas a divider less FS eliminates power hungry dividers of frequency plays as a foremost solution for low power and in all the integrated systems. The phase of the reference signal and the value of the VCO output of the reference signals is compared with the aperture phase at every edge of rising stage. This will be a small fraction of the reference period. This idea is suitable for systems which require only one LO signal. It has a major limitation as that it cannot be applied to wireless systems which uses multiple LO frequencies having a small frequency separation.

The synthesizer building blocks are comprised of major parts such as Injection-Locked Frequency Divider and voltage controlled oscillator, Pulse Swallow Frequency Divider, Charge Pump and loop filter. The VCO is used for quadrature signal generation. It is also used for lowpower frequency dividers with multi-channel selection process. The locked divider used in frequency synthesizer system is designed to find the accuracy of the frequency output under many operating conditions. In FS the critical parameter performance is phase noise. One of the main aim to achieve this phase noise is by fine frequency resolution. The device employed in this process is Ultra low power CMOS PLL synthesizers. The power consumption should be of reasonable levels. Due to this nature, it has been a challenging task for all the designers. Our contribution of this paper is:

1. A conventional PD in the circuit is replaced by XOR-PD. Whereas the phase difference in the inputs can be obtained easily by XOR-PD.
2. In this paper, an overall low power pahse noise quadrature cross-coupled 1.8GHz VCO design, featuring a power consumption of just 20 mW is utilized. It is very low power consumption and low phase noise due to Low power VCO design structure [17].
3. In this paper, it is carried out a detailed system for reducing the power consumption on the dynamic logic circuit. It is considering the digital dividers and the low power prescalers in the circuit system. This is system is focused for IEEE 802.1X.X applications.
4. Also a phase noise reduction and power consumption of the CMOS VCO is obtained by a low power cross coupled LC-VCO with optimized phase noise.

II. RELATED WORKS

Few recent researches were tried with different approaches, techniques for frequency synthesizing. Some of them are: 60 GHz – 5Gb/s QPSK transmitter with on-chip T/R switch and fully differential PLL frequency synthesizer [2], FMCW-[Frequency Modulated Continuous Wave] radar [3] operating based frequency synthesization, high sensitive CMOS-based sensing the frequencies [4], Single PLL for simultaneously locking two mixing oscillators [5], Fast High precision VCO frequency calibration technique [6], PFD combined CP in PLL [7] and SHIL Fractional N-frequency synthesizer [8]. It provides spread spectrum and low power RF technology is implemented in bipolar technology. In an integrated CMOS VCO design, large output voltage swings are usually favorable to improve the oscillator phase noise and mixer noise figure (NF). However, the poor –factor of CMOS on-chip inductors results in an inefficient usage of power [9]. In this paper an integrated CMOS VCO design, to improve the oscillator phase noise large output voltage swings are usually favorable. But the CMOS power factor results in an inefficient usage of power. In this proposed work some inductors of high off chip are used up to implement a low power VCO of high performance. Due to the relaxed budget link the receiver could tolerate a much amount of decibels. Thus the high chip inductors helps in optimizing the low phase noise, including minimum currents and to mix the driver it need to produce necessary voltage [10].

Another approach is also discussed in order to improve the power consumption is by using the injection locked oscillator. It has also been used as a frequency divider. This is able to provide a divide-by-two circuit which is of high speed with low power consumption when compared to its digital counterparts [11]. In this approach a 1-V high speed frequency divider is proposed. It employs a common gate topology. The operating frequencies up to 5.2 GHz are estimated with the small signal analysis. [12].

For reducing the power consumption the dynamic dividers in CMOS phase locked loops are adopted for multi Giga hertz application. It doesn't affect the phase noise and power supply of the phase locked loop. The PLL has been used up in wireless LAN applications. It can synthesize frequencies in the range of 5.14 to 5.70 GHz. So divide by two flip-flop operating up to 5.2 GHz CMOS technology was achieved [13]. The CMOS varactor is used as an MOS capacitor for accumulating the depleting mode. This is used only because of its better factor. This results in a lower up converted phase noise. In spite of its lower mobility, the design is favored because of its noise considerations [14]. The focus of this paper is an implementation of prescaler and the phase detector. The frequency synthesizers are required by the wireless standards which are derived from the specifications. Finally the implementation alternatives of the synthesizer's blocks are under review [15]. As it is noted in this paper the role of frequency synthesizer provides a reference signal with a proper frequency such that modulated information is converted into a signal. This

will be of lower frequency As it is noted in this paper, the dual band frequency synthesizer in 0.35µm with integrated CMOS technology was introduced. It achieves a phase noise in PCS band and the fractional spurs are reduced.[16]. The ROM lookup table was replaced by the DAC digital to analog converter to implement FS was proposed in order to improve the power saving strategy. By using one nonlinear resistor of the string mode DAC and current mode DAC are used. Thus, it results in power dissipation of 4 MW and 92 MW at respective frequencies 25 and 230 MHz even for a 3.3 V supply [17].

The new method of design is proposed which merges both the sine and cosine lookup tables with the CORDIC- interpolation to get a hybrid architecture. This design optimization of the LUT/CORDIC ratio reduces the power and silicon area for a particular clock frequency [18].

The new design method is proposed in the paper in which higher compression in the ROM is achieved. It also implements 48 bits frequency control which results same spurious level. It analyses the phase truncation effect and techniques to overcome. By this method the frequency resolution is generated in the sub hertz range [19]. Monolithically integrated W-band two frequency synthesizers are implemented. Injection locked frequency tripler and harmonic based frequency tripler are employed. These are suitable for integration in millimeter phased array and in wireless communications multi pixel systems [20].

The synthesizer proposed in the paper adopts integer-N architecture with reference of 50-MHz. The phase rotation provides the beam forming capability for the transceiver. The frequency synthesizer embedded in the design occupies less space and consumes less power thus leading to optimization [21].

A low power PLL frequency synthesizer with fast settling was incorporated in this approach to work at 1.72 GHz for 100 KB/s. Also a dynamic bandwidth scheme adds to it to meet the time division requirements with half duplex wireless systems [22]. A frequency synthesizer with 60 GHz with a in phase injection coupled quadrature VCO is proposed. This compact design reduces both the phase noise, error and the power consumed. This was implemented in the low power CMOS technology [23].The approach is based on a design which focus on the VCO with a lower power and minimum phase noise bond and loop bandwidth technique. By this the speed of PLL frequency synthesizer was easily determined. A novel lock detector was enabled to control the bandwidth [24].

III. PHASE LOCKED LOOP FREQUENCY SYNTHESIZER

A set of sinusoidal signal is generated by the frequency synthesizer at a defined frequency, and it has predefined stability and precision. Figure-1 shows the common architecture of a present transceiver [25]. The resulting signal generated by the FS is normally known as the local oscillator signal, where it can be used as reference for frequency translation and channel selection in communication systems.

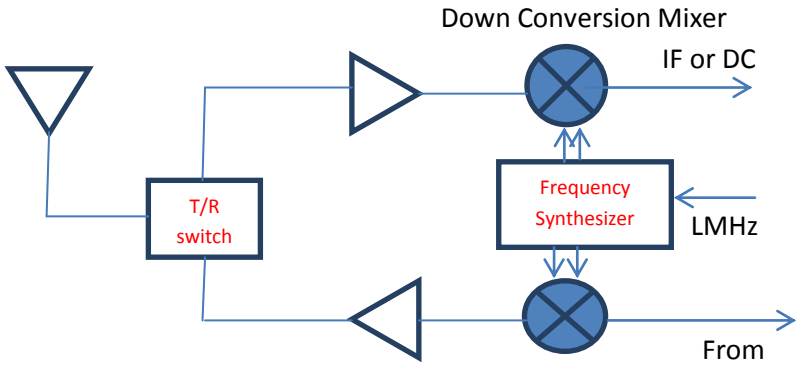

Figure-1: Role of Frequency Synthesizer in a Transceiver

To convert the incoming signals in the receiver side, the high frequency LO signal is used to change into lower frequency signal and it will be processed to extract information carrying by the signal. At the same time the same LO signal is used to convert the up-signal to an RF frequency, thus it can be transmitted over the medium. Our frequency synthesizer is mainly used to ensure the accuracy of the output signal under the operating given conditions. PLL is used to implement the frequency synthesizer normally.

A. Phase Noise

A stable channel frequency can be provided by a frequency synthesizer, and it should be a single tone at the preferred frequency. A delta function in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain. Due to random amplitude and phase deviations the preferred frequency values produce energy in the side-bands. While mixing this energy with the received modulated baseband signal, undesired sidebands are created. The performance of the waveform is indicated by two parameters as phase noise and spurious tones. Phase noise makes the higher frequencies into weaker frequencies.

IV. PHASE LOCKED LOOP

Phase Locked Loops are most generally used to design the frequency synthesizer of radio frequency transceivers. In this paper, we start explaining from phase locking. Consider two signals

$$x_1(t) = \cos(\omega_1 t + \emptyset_1 t)$$

and

$$x_2(t) = \cos(\omega_2 t + \emptyset_2 t)$$

are two instant phases: and the Frequencies are:

$$\beta_1(t) = \omega_1 t + \emptyset_1 t \text{ and } \beta_2(t) = \omega_2 t + \emptyset_2 t$$

$$\Omega_1(t) = \delta[\beta_1(t)]/\delta t = \omega_1 + \delta[\phi_1(t)]/\delta t$$
$$\Omega_2(t) = \delta[\beta_2(t)]/\delta t = \omega_2 + \delta[\phi_2(t)]/\delta t$$

The phase difference between two signals is constant with time is negligible is termed as phase lock. So that, during the locked condition,

$$\beta_1(t) - \beta_2(t) = constant$$

$$\frac{\delta[\beta_1(t) - \beta_2(t)]}{\delta t} = \omega_1 - \omega_2 = 0$$

Which indicates that if the loop achieves locking, no frequency difference between two signals during comparison. But, using feedback loop, the constant phase difference of two periodic signals is ensured when the loop reaches its steady state.

V. PLL FUNCTIONALITY

The entire functionality of the PLL is illustrated in Figure-2. Since, PLL has been a feedback system, it can minimize the phase difference between the reference input [f_{ref}] and feedback signal [f_{div}]. Also a phase detector [PD] generates a phase error where its DC value is proportional to the difference between the phases of the reference and feedback signal. The low pass filter extracts the DC value and applied it to the VCO, and it changes the output frequency f_{out}. The frequency synthesizer divides the output frequency in to N division and employed the signal by comparing with the input frequency.

There are three types of PLL are: Type-1 PLL, Type-2 PLL and Type-3 PLL. From the PLL discussion, the output frequency of the PLL is programmed by setting the frequency division ratio with various values. Indeed, the PLL based frequency synthesizer is mostly used in modern wireless communication systems.

A. Low Power PLL Frequency Synthesizers

In the first stage of building a low power frequency synthesizer a prescaler is assigned in the synthesizer block. Because, the preschooler can work at higher frequency and it is used to reduce the power utilization. In our block design the state-of-the-art CMOS N/(N+1) prescalers have been used with different topologies such as injection-locked frequency dividers (ILEFDs), current-mode logic latches and dynamic logic circuits.

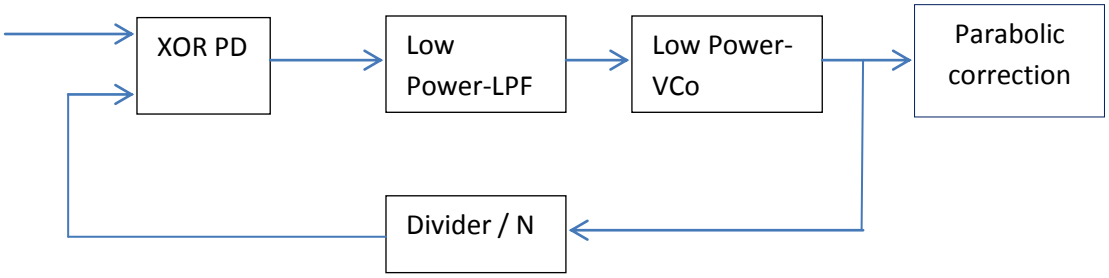

Figure-2: Proposed PLL Structure

VI. BUILDING BLOCKS OF FREQUENCY SYNTHESIZER

A. *Phase Detector or Phase Frequency Detector [PD/PFD]*

Phase detector is a circuit its average output (V_{out}) is proportional to the phase difference $(\Delta\emptyset)$ between its two inputs. In certain case, the association between $\overline{V_{out}}$ And $\Delta\emptyset$ is linear, and it crosses the origin as $\Delta\emptyset = 0$. The gain of the PD is represented as V/rad.

B. *PD Based on XOR*

One of the famous PD is the exclusive OR gate illustrated in Figure-3a. The phase differs in term of input variation, the width of the output pulses provides a DC level which is proportional to $\Delta\emptyset$. The XOR-PD produces error pulses on both rising and falling edges. Figure-3c shows the transfer characteristics of the XOR-PD.

One of the main drawbacks in XOR-PD is it not able to detect the frequency variations. If any frequency variation exists the phase difference will be accumulated either in a positive direction or in a negative direction. Figure-3c the transfer function of PD is symmetrical over Y-axis due to which it fails to differentiate the polarity of the phase difference, and thus the frequency difference. The second issue is that, when the PLL is locked, the average of XOR PD output is zero. This zero voltage is averaged from a square wave of twice the reference frequency. Therefore, the pole of LPF has to be low enough to attenuate this reference spur. The XOR PD is sensitive to the duty cycle of the input signals.

C. *Design of low power LC VCO*

The channel frequencies should be synthesized for IEEE 802.1x.x standard applications under the spectrum of $2400 - 2483\ MHz$. 83 MHz is the minimum tuning range required for the VCO of the proposed model. To correct the parabolic formation and the other relevant issues the tuning limitations are restricted to lesser than 250 MHz where the sensitivity (K_{vco}) is very small. This small sensitivity value of the VCO can control the phase noise, and smaller loop filter capacitance and degrade the phase noise performance.

Figure-3(a): XOR-PD

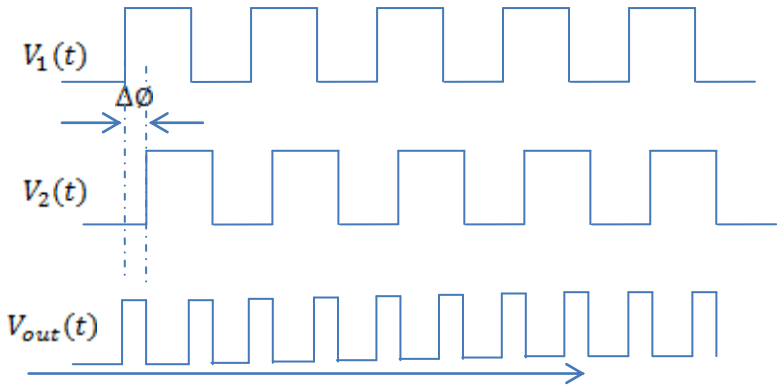

Figure-3(b)

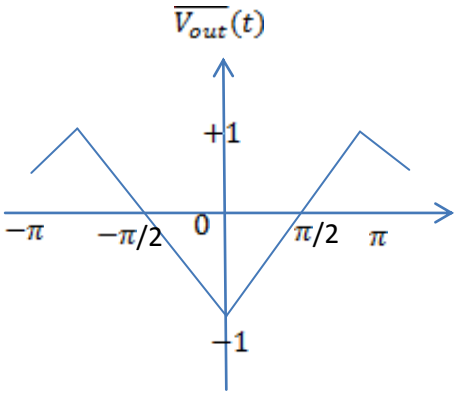

Figure-3(c)

D. Parabolic Based Wave Correction

There is a close resemblance among sine wave and parabolic wave. Quadratic polynomial –ax2 + bx + c is considered to approximate the parabola. The time axis [X-axis] is segmented into 2N-1 segments. Thus, the addresses required from phase accumulator start from 0 to 2N-1. To reduce the complexity, of the arithmetic scaling, a=1, b=2N-1 and c=0 are assigned. N is mostly assigned as 12 or 8 due to the 12 bit or 8 bit DAC is readily available in the market.

The final equation becomes n(n-2n-1) or –n(2n-1-n), where n is assigned as an integer from 0 to 2n-1. So the parabola has become a zero value of 0 to 2n-1. The vertex or the highest peak amplitude of the parabola is given by –D/4a. Where D=b2-4ac.

In our simulation based experiment in MATLAB, it is considered that N=10, it gives the maximum number of samples of the parabola is 1024. Polynomial n(1023-n) is assumed for reducing the complexity as the parabola will form on the first quadrant of two dimensional Cartesian coordinate system. The 10 digit addressing, with 0 to 1023 integers based abscissa is also compatible with available DACs.

There are two factors are taken from the equation n(2n-1-n) are n with [(2n-1)-n] and 2's compliment of a [6] is multiplied by n gives parabolic polynomial. This important scaling is an essential factor. The 8-bit address line of the phase accumulator is increased into 10-bit address help to increase the phase values. The increased 10-bit addresses maximize the samples from 256 into 1024 for every half cycle. The half sine wave, thus generated from the parabolic approximation which is shown in Figure-4.

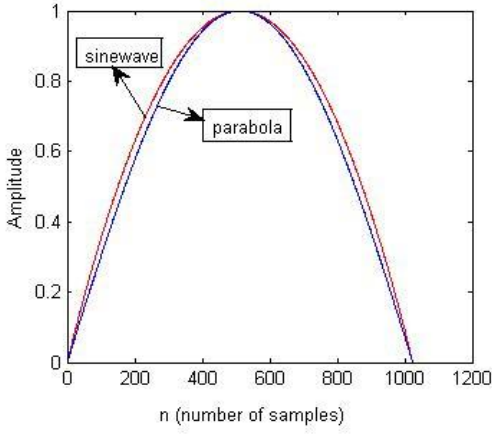

Figure-4: Plot of half sine wave and parabola

The parabola shown in Figure-4 is differing from the half sine wave. The difference between the parabola and half sine wave can be obtained by subtracting the parabola from the half sine wave. Figure-4 shows the thorough investigation of the vertical symmetry, that the error is more in the middle of the quarter wave and less at the top and bottom of the quarter curve. The error curve is illustrated in Figure-5. The error signal is given in the equation – (1) as:

$$Error = [n(2^N - n) \div 262144 - sin\frac{2\pi n}{T} for 0 \leq n \leq 2^n$$

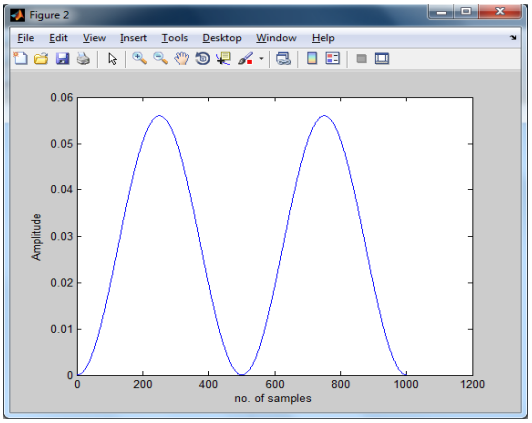

Figure-5: Error between the Parabola and half sine wave

VII. MODIFICATION OF PARABOLA AND ARCHITECTURE

The observed error curve is depicted in Figure-5, which indicates that the error curve is a multiple curves similar to a parabola with asymmetric in nature and the sample values of a parabola are greater than the sine wave and non-uniform in nature, through a quarter cycle. The error curve is linearly approximated and found a curve similar to triangular wave with different slopes as shown in Figure-6. It is observed that first and fourth line has the same slope in magnitude, whereas second and third have different slopes in magnitude.

In addition to the availability, the curve in Figure-6, is modified into double triangular wave with a slope of 0.56/256 for all, n/4 segments and then-bits are taken in creating the parabola. To make more simplification of arithmetic of addressing, the curve in figure-6 is modified further to a double triangular wave with a slope of 0.112/256 for all, n/4 segments, where n-bits are taken

for forming parabola.

This curve indicates that the value of n from 0 to 255, 255 to 512, 512 to 768 and 768 to 1023 has been defined for the function of

$$\frac{112}{256000}x, \frac{112(513-x)}{256000}, \frac{112(x-513)}{256000}, \frac{112(1023-x)}{256000}$$

respectively with a slope of 0.112/256.

VIII. SIMULATION RESULTS AND DISCUSSION

The block is created in MATLAB Simulink model used to implement the proposed low power, less complexity PLL for CMOS in terms of frequency synthesizer, where it includes the parabola generation scheme and it is evaluated by investigating various parameter variations and the effect on the parabola. The circuit is also implemented by developing a Simulink model and the results are verified. From the results it is observed that the error before modification, the peak magnitude is 0.56 and after correction the peak magnitude is 0.0286. All the frequency is controlled at 01 and changing N from 8 to 16 in steps of one's and it does not affect the error. Also easy to understand and verify the error model is assigned with a fixed error value and the error curve is depicted in Figure-8.

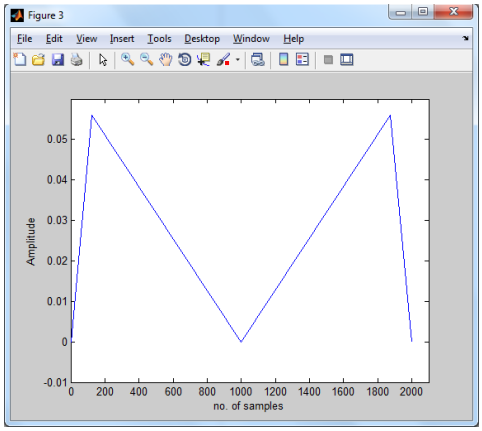

Figure-6: Approximated Error Signal into triangular wave

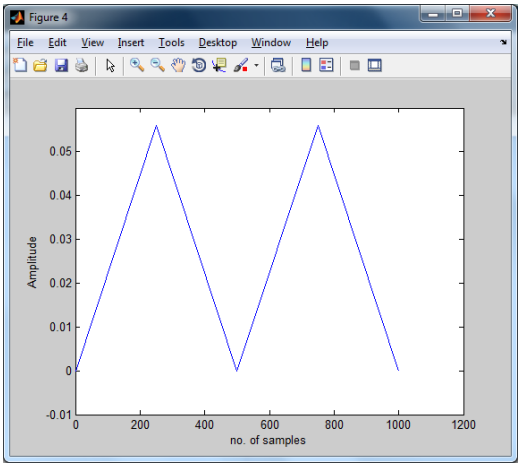

Figure-7: Modified Double triangular wave

From this figure, it is clear that the curve swings available between +0.0286 to -0.0056 with the mean absolute error 0.0115. The modified parabola is compared with the pure sine wave. It is obtained by the sine wave formed with the help of the modified parabola with the pure sine wave and since wave formed with the help of pure parabola is depicted in Figure-9. The pure parabola, modified parabola and pure sine wave are indicated in red, blue and green respectively for easy verification.

The power spectrum is also checked and FFT of the sine wave by the modified parabola is given in Figure-10, where it is almost same as pure sine wave. Further the SFDR performance of the sine wave with the help of modified is 106dBc.

Table-1: Performance Comparison in terms of SFDR

Approaches	SFDR [dBc]
Quadrature [25]	75
Parabolic[25]	102
Our Approach	106

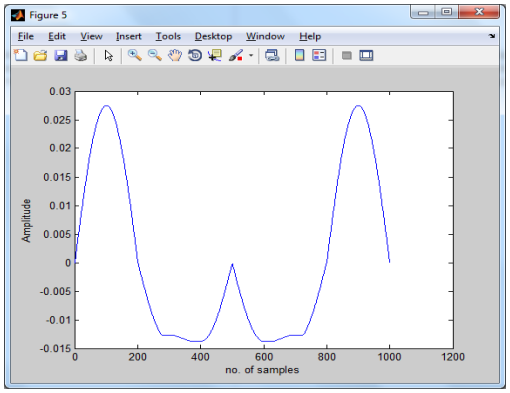

Figure-8: Final Error Curve

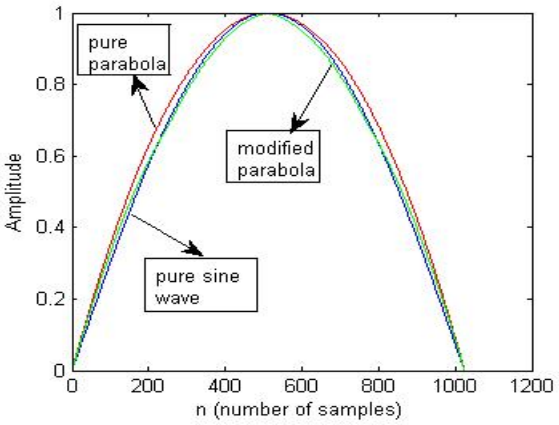

Figure-9: pure and modified parabola

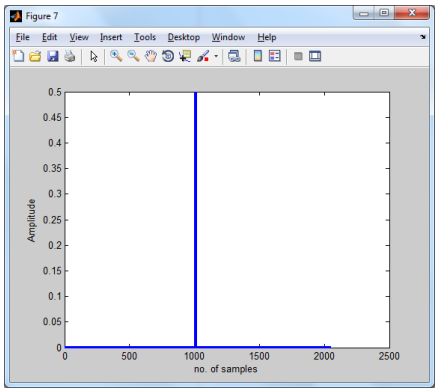

Figure-10: FFT of sine wave by modified parabola

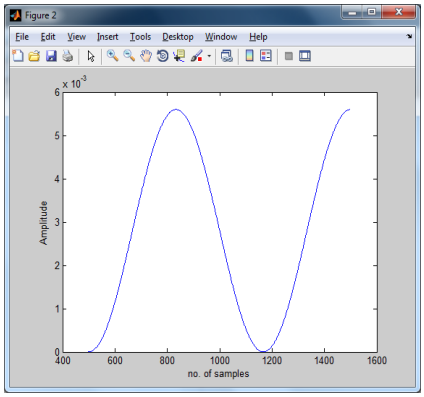

Figure-11: Final Error Model

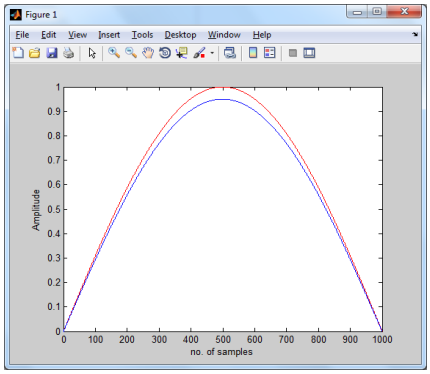

Figure-12: Obtained Pure and modified parabola

Our proposed model consumes more power than the existing approaches and methods. Because of the low power prescaler, low power building blocks, low spur gain boosting charge with low power VCO with the suppressing noise in tails, our synthesizer consumes 1.8 mW of power measured from our experimental results

IX. CONCLUSION

In the previous systems or the approaches suffers some accuracy. In our system, all the relative components and their advantages can provide better performance in terms of accuracy, speed, logistics and own applications. The experimented results in Figure-11 and Figure-12 shows the efficiency of our proposed model. The perspective of our proposed design is to remove the look-up-table and reduce the complexity in terms of hardware, memory usage, and low power utilization with appropriate accuracy in terms of dBc. It is proved from the following table that the main objective of the design is met.

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