FIN-FET TECHNOLOGY FOR ULTRA LOW POWER DESIGN

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ABSTRACT

In this paper we first explore the sub-threshold conduction and region. Our analysis indicate that the energy consumption is very less in Fin-FET than CMOS technology in sub-threshold region. In the paper it is also concluded that by using pull down network the power consumption can be reduced further. By using Fin-FET domino logic the technology is scaled down to the 33nm and delay in the circuit is also reduced.

I. INTRODUCTION

The term Fin-FET was coined by University of California, Berkeley researchers (Profs. Chenming Hu, Tsu-Jae King-Liu and Jeffrey Bokor) to describe a non-planar, double-gate transistor built on an SOI substrate. Fin-FET is used extensively for its some features like scale down of CMOS technology and for the less power consumption. For some application like wireless devices, medical devices and sensors network nodes we require low energy consumption with the desirable speed. Energy consumption is minimum in sub-threshold region[1].

The sub-threshold region is often referred to as the weak inversion region, and sub-threshold conduction of transistors has been very small, but as transistors have been scaled down, leakage from all sources has increased. The reason for a growing importance of sub-threshold conduction is that the supply voltage has continually scaled down, to reduce the dynamic power consumption of integrated circuits.

There are some approaches used for dynamic control of threshold voltage; includes dynamic-threshold voltage MOS(DTMOS)[2],body biasing[3], and multiple threshold CMOS(MT-CMOS)[4]. Double gate Fin-FET is best for the lower power consumption application.

In this paper we will discuss about ultra-low power design for Fin-FET circuits. Our analysis show that Fin-FET circuits have lower functional supply and lower energy consumption in comparison to CMOS in sub-threshold region.

II. Fin-FET TECHNOLOGY

A. Fin-FET Structure

Figure 1 shows the structure of Fin-FET device.[5] .In these circuit (T_{si}) is the thickness of find (H) is the height of the fin.

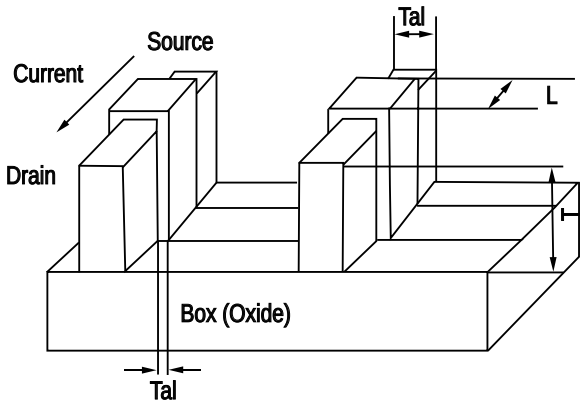

Fig. 1. Fin-FET structure

B. Fin-FET Technology

It is a vertical double gate device and it is alternative device for sub-45nm.[6]. Fig shows the 3D structure of Fin-FET [7] .

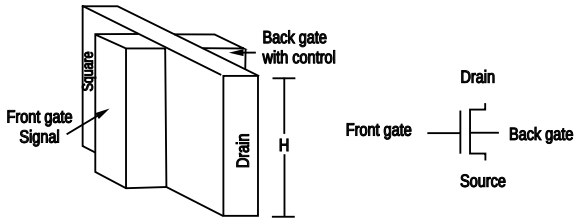

Fig. 2. FinFET structure and symbol

C. Sub threshold circuit

In sub-threshold region, energy dissipated in circuit is

$$E_{\text{active}} = \alpha\, CV_{dd}^2$$

α is activity factor, C is total switching capacitance, V_{dd} is the power supply and sub-threshold current is

$$I_{sab} = Ke^{\frac{V_{gs}-V_{th}}{nV_T}}\left(1-e^{-\frac{V_{ds}}{V^T}}\right)$$

Where k is technology related factor,V_T is the thermal voltage.[1]

D. Methodology

One method is defined in paper[1],for determining the dependency of energy on supply voltage is use 30-stage inverter chain and 8-bit ripple carry adder. Adder is used to finding the delay in worst case which is least bit carry to maximum bit sum.

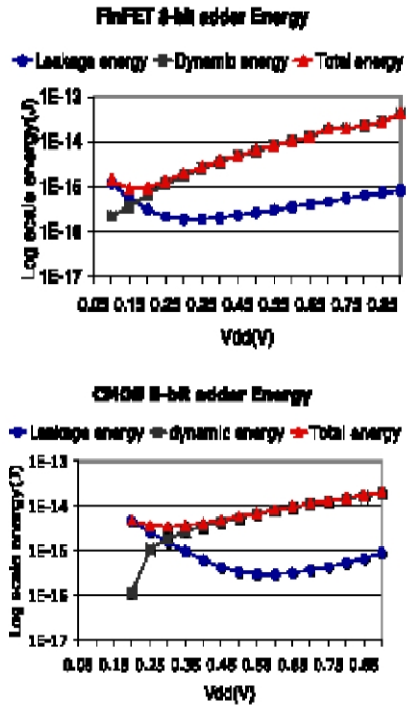

Fig. 3. Fin-FET and CMOS 8-bit adder energy

Fig 3 shows that leakage energy is continuously decreasing as we reduce the sub-threshold voltage means that as we boost dynamic power leakage energy is decreasing means here conservation of energy principle is applied[1].Minimum energy point for 32nm Fin-FET inverter chain is obtained at 120mv and 230mv is obtained for 32nm CMOS inverter chain[1]. when the voltage is below 150mv Fin-FET is working but CMOS inverter chain will not work. it shows that Fin-FET can be used below threshold level or under 50mv power supply[1].

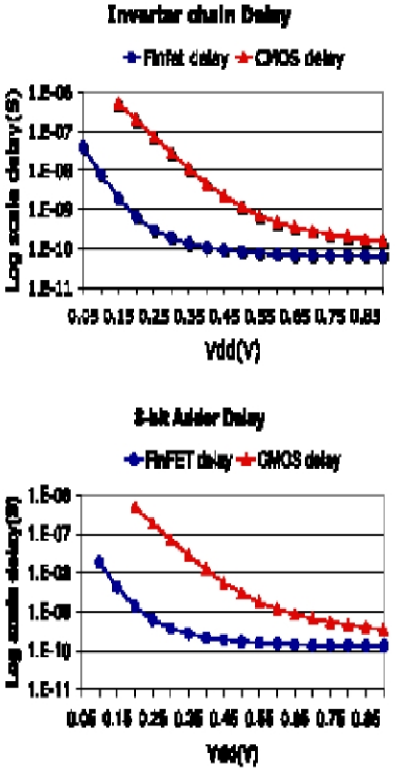

Fig. 4. Voltage Vs delay

Fig. 4. shows that for same power supply voltage delay is smaller in Fin-FET as compared to the CMOS circuit.[1] .

III. DISCUSSION

In the following fig Fin-FET circuit with the CMOS technique is compared for the power consumption in 32 nm Fin-FET technology using Taurus-Medici [8].

As shown in the fig.5 by using Fin-FET domino circuits the power consumption is reduced up to the 55% than other domino circuits. But these power consumption can be further reduced upto 5% by using pull down network as compared to the Fin-FET domino logic.[8]

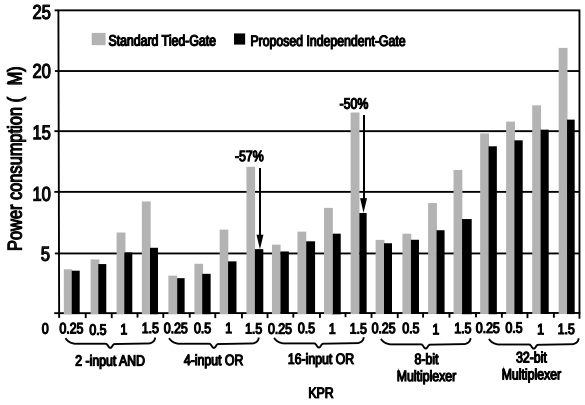

Fig. 5. Logic gates Vs Power consumption

According to the authors view in the Fin-FET domino logic we used two gates in the circuit for controlling the circuit, by that we can operate the FET in sub-threshold region which is not possible with the single gate by which power consumption is reduced up to the desired level. So in my view if we work further in the field in which more than two gate or multi gate device is used power level can be reduced further.

Another view is that the problem with the sub-threshold region is management variability. To do work in sub-threshold region is complicated because it is very low voltage. So further innovation should be done in these field.

IV. CONCLUSION

In these paper we studied that double gate MOS-FET is best suited for technology scaling. We have also seen by the experimental data that the power consumption for the Fin-FET circuit is very less in sub-threshold region. By using Fin-FET transistor size can be reduced up to 33nm.Hence Fin-FET is most suited for scaling and ultra low power design. But sub-threshold region is very low voltage region so do work in it is very difficult so further innovation should be done in these.

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