Periodic Wave Generation for Direct Digital Synthesization

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Abstract

From the oscillators to PLL, various methods have been introduced to improve the stability, frequency resolution and spectrum purity. Among the all-digital approaches, Direct Digital frequency synthesis is considered as main. The main objective of this paper is to improve the output signal quality. Nowadays modern system designs needs to improve the quality of the waveform generated. An overview of the fundamentals of DDS along with the formulation to compute the bounds of the signal characteristics are resented here. Also two different quantization methods are used to synthesize the output waveform. Several methods, patented are presented in the earlier research works to overcome the limits of the basic DDS in terms of improving the quality of the output signal. But in this paper, there are two stage of task is applied with two different quantization methods for improving the accuracy in terms of signal Synthesization.

Keywords: Type your keywords here, separated by semicolons ;

I. INTRODUCTION

Frequency synthesis is the process of deriving a new frequency from fundamental frequency. In other words it is a frequency changing process done by the combination of addition, subtraction, multiplication and division process. It is a vital component of modern wireless communication system. Hence if there is any change in frequency synthesizer it will directly affects the quality of the wireless communication systems. At present it also acts an important role in radiofrequency development and equipment. It is generally divided into Direct and Indirect Frequency synthesizer. Direct frequency synthesizer creates frequency waveform directly from fundamental without any form of frequency transforming elements. It is further classified into Direct Analogue Frequency Synthesization (DAFS) and Direct Digital Frequency Synthesization (DDFS) [1]. DAFS has excellent switching time performance but it consumes more power due to the integration of mixer, filter and other components. Hence it is also called as mix-filter-divide architecture. DAFS has various drawbacks such as it contains large number of spurious signal and this can be eliminated only by adding filtering which further increases the cost of the system. Due to these reasons DAFS is selected as a last alternative when compared with the other forms of frequency synthesis. DDFS has a higher switching frequency time with low phase noise and extremely tiny resolutions [2]. The main drawback of DDFS is that it can't generate high output frequency. The indirect frequency synthesizer generates output frequency indirectly based on phase locked loop technology. In order to obtain high stable output frequency reference frequency is used to indirectly control the VCO output. Since the output frequency generated by the oscillator is not controlled directly it is named as indirect frequency synthesizer. When comparing with other schemes PLL based frequency synthesizer, indirect frequency synthesizer has a wide range of output and higher suppression of spurious signals. It is further classified into two indirect analogue frequency synthesis (IAFS) and indirect digital frequency synthesis (IDFS) [6]. Indirect analogue frequency synthesis (IAFS) uses PLL technology with a mixer placed between the VCO and phase detector. This enables the offset frequency to be introduced into the loop. The indirect digital frequency synthesis (IDFS) technique introduces a digital divide into the phase locked loop between the VCO and the phase detector.

The VCO runs at a frequency equal to the phase comparison frequency times the division ratio hence by altering the division ratio the frequency of the output signal can be altered. The PLL based frequency synthesizer [3] comprises of both high and low frequency

blocks. A typical PLL based frequency synthesizer comprises both high and low frequency blocks. High frequency blocks consists of mainly the VCO and first stage of the frequency dividers are the main power consuming blocks, especially in a Complementary Metal Oxide Semiconductor (CMOS) implemented frequency synthesizer. Implementation of CMOS become a cheaper alternative to other commercially available IC due to its advances in CMOS fabrication have achieved frequency range greater than 50 GHz. Though cost is high this solution is suitable for many applications.

In all the communication systems the major block behaving as a well- controlled signal source is the frequency synthesizer. It plays an important part in the frequency modulated continuous wave radars [5]. These synthesizers have been used up in Si based semiconductors technology. The direct digital frequency synthesized type is better than the CMOS type in terms of power consumption and size of circuits. The Direct Digital Frequency Synthesizer is an electronic device [1] which generates discrete samples from a single source or from multiple sources and converting them to different frequencies sine wave by keeping the reference frequency as the base. This uses digital data and signal processing blocks to generate a waveform. This has a provision of fast switching, linear phase and shifts in frequency over a wide range of frequency. They find its application in wireless transceivers, clock generation and modulation due to its large scale integration implementation solutions. The benefit is that the phase amplitude and output frequency are manipulated. It could hop between frequencies by tuning with fine frequency and phase resolution.

A. Related Works

One of the inspiring problems not fully addressed because of fundamentally non-linear nature of the synchronization occurrence [7 – 10] and to the lack of a simple and accurate analytical model for ILFDs, especially in the case of direct injection RFDs [4]. Contributions to this problem based on analytical approaches are already discussed in [11] aimed mainly at the prediction of the locking range. Various modulation capabilities are included due to its digital nature. A high degree of system integration can be achieved. It has a fast switching frequency, low noise, better resolution thus it is hugely applied in modern communications. Thus it finds itself better than PLL. DDFS are taken as the alternative to PLL in communication systems such as mobile, satellite communication. The frequency generation is 1/3rd of the reference frequency.

In our paper, the waveform is considered as a sine wave referred from [2]. It may be a square wave, a triangular wave, saw-tooth wave or any periodic waveform. It is assumed that the sampling frequency Fs is a known constant. Before going for implementation let summarize the DDS value. To satisfy most of the design specifications, the tuning resolution should be made arbitrarily small. Within one sample period, the frequency and the phase is controlled to do modulation as feasible. To do DDS implementation integer arithmetic is used in any microcontrollers. DDS implementation is always stable, having finite length of control words. There is no need for an automatic gain control. Whenever the frequency is changed, the phase continuity is also changed.

B. Implementation of DDS

Frequency Synthesization use DDS technique for generating sine waves in specific frequencies. Digital circuits are used to generate the analog waves here. In reference to the clock frequency the quantized digital samples are generated. Then the digital sample based waveforms are converted into analog signals using D/A converters and filter circuits.

There are two different stages of task is taken for implementing DDS which is shown in Figure-1. The first stage task is the accumulator which is outputting a phase value ACC and a phase to waveform converter outputting the desired DDS signal.

C. Sampling Frequency to Phase

It is well known that integer arithmetic is used for DDS implementation. It is considered that the accumulator size is $\boldsymbol{N\ b}$. The period applied for the output signal is $\boldsymbol{2\pi}$ radius, the maximum phase is represented by the integer number is $\boldsymbol{2N}$. $\boldsymbol{\Delta_{ACC}}$ Denotes the phase increment related to the desired output

frequency F_o. It can be coded in the form of integer is $N-1$ b.

At the time of one sample period T_s, the phase increases by Δ_{ACC}. So that, it takes T_o to reach the maximum phase 2^N:

$$T_o = \frac{1}{F_o} = \frac{2^N T_s}{\Delta_{ACC}} \qquad (1)$$

It can be rewrite (1) in term of frequency F_o, as a function of Δ_{ACC} :

$$F_o = F_o(\Delta_{ACC}) = \frac{F_s}{2^N}\Delta_{ACC} \qquad (2)$$

The phase incrementΔ_{ACC}, rounded to the nearest integer ($\lfloor x \rfloor$) is the integer part of x is given by

$$\Delta_{ACC} = \left\lfloor F_o \frac{2^N}{F_s} + 0.5 \right\rfloor \qquad (3)$$

Equation (2) is the basic equation representing any DDS system. From (2) one can infer tuning step in frequency ΔF_{omin}, which is the smallest step in frequency, which the DDDS can achieve:

$$\begin{aligned} \Delta F_{omin} &= F_o(\Delta_{ACC}+1) - F_o(\Delta_{ACC}) \\ &= \frac{F_s}{2^N}(\Delta_{ACC} + -\Delta_{ACC}) \\ &= \frac{F_s}{2^N} \end{aligned} \qquad (4)$$

Equation (4) allows the designer to choose the number of bits 9N) of the accumulator ACC. This number N is often referred to as the frequency tuning word length [6]. It is calculated from:

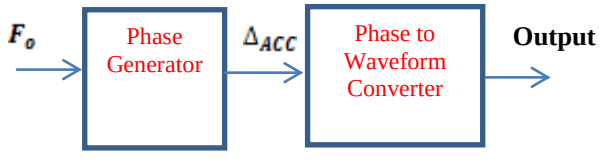

Figure-1: DDS Process

$$N = \left\lfloor log_2\left(\frac{F_s}{\Delta F_{omin}}\right) + 0.5 \right\rfloor \qquad (5)$$

For the minimum frequencyF_{omin}, the DDS can generate the smallest phase increment with $\Delta_{ACC} = 1$ in (2), and still it increases the phase, but $\Delta_{ACC} = 0$ does not increase. F_{omin} can be written as:

$$F_{omin} = \frac{F_s}{2^N} \qquad (6)$$

For the maximum frequency F_{omax}, DDS can generate the uniform sampling as:

$$F_{omax} = \frac{F_s}{2} \qquad (7)$$

From the experimental point of view a lower F_{omax} is often preferred $F_{omax} = \frac{F_s}{4}$ is the example. The lower output frequency of the analog reconstruction is obtained by a low pass filter.

D. Advantages of DDS

DDS has the ability to provide fast frequency switching at a stumpy rate. The waveform frequency is adjustable in micro hertz based frequency resolution. It also helps to adjust the phase and amplitude digitally. The core of the DDS can also be combined with additional signal processing blocks to make clock generators.

II. Phase to Waveform Generation

From the above description and formulas phase is generated from the sampling frequency. Now the waveform is generated from the phase. The code is N b in the accumulator. The waveform can be defined up to 2^N phase values. If 2^N is too big for implementation, the phase to amplitude converter is used to reduce fewer bits from N. Let we consider that P is the number of bits used in the phase generation where P$\leq N$. The output waveform values can be stored in the look up table for further processing with 2P series.

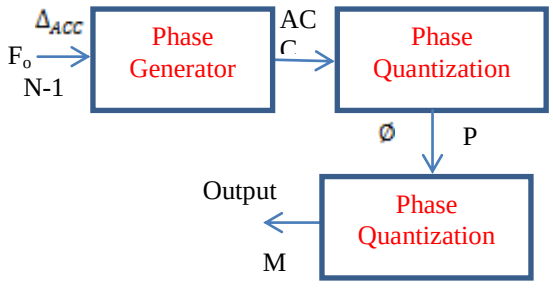

Figure-2: Signals Generated by DDS

Figure-2 shows the implementation of the second stage task of the proposed approach. It shows that the other output waveform generation techniques are based on the approximation methods. DDS generates a sine wave where the offset value is b and a peak amplitude value is a. The content of the look up table is the output values of the DDS. This output value is computed using the index value i ranging from 0 to (2^P -1).

$$LUT(i) = \left\lfloor \left(b + a \sin\left(\frac{2\pi i}{2^P}\right)\right) + 0.5 \right\rfloor \quad (8)$$

Using the LUT computation, for example some specific values P=9, a=127.5 and b =127.5 and the output waveform for $F_s = 44$, 100 Hz and $F_o = 233$Hz is plotted as the back curve in Figure-3. It also can be used to generate two quadrature signals by applying two important things. One is to read the LUT(i) and the other is LUT(i+2P/4) which will be converted into corresponding sine and to the cosine functions. A square wave form is already available, and the most significant bit of the phase accumulator ACC is shown in red curve in figure-3. The MSB toggles every π radius, because of the accumulator represents **2** π radius. It is point out that this square wave is corrupted due to jitter [3] of the sampling period Ts. This phase jitter occurs due to sampling scheme used to synthesize the waveform.

The output of the DDS can occur only at a clock edge. If the output signal is not generated by the DDS then a phase error will occur and increases slowly between the ideal output and the actual output until it reaches one clock period. Again it starts increases when the error returns to zero [4].

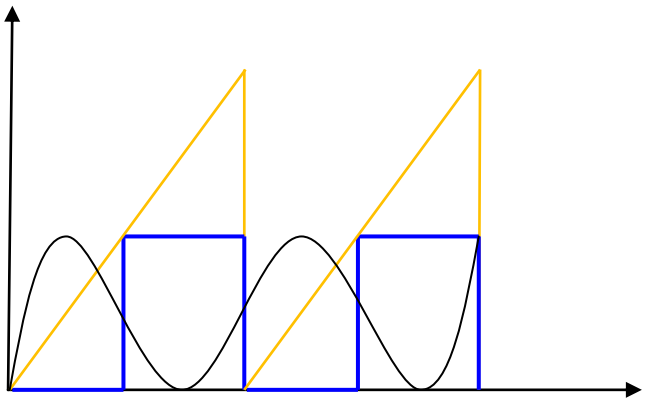

Figure-3: Signals Generated by DDS

A saw tooth signal is also available with no computational overhead. The linearly increasing phase accumulator ACC value is stored modulo 2*N*, thus leading to a saw tooth signal as shown by the blue curve in Figure 2. The LUT is not used in this case, or it is the identity function: Output=ACC. With the use of logic gates, a triangular output waveform can be generated from the saw tooth.

III. SIMULATION RESULTS

The performance of the DDS at various frequencies is verified by setting the following parameters in the MATLAB software. They are:

Table-1: Parameters Used for Simulating DDS

Parameter	Value
Sampling Frequencies	60 MHz
Frequency Tuning Word	11 bit
Phase Tuning Word	9 bit
Output Amplitude Tuning Word	16 bit

All the above parameters with some more additional parameters are assigned in a text file and input to the MATLAB which read this file by test bench from ISE. The suitable design parameters for DDS module is assigned in the Following Table-2.

Table-2: Performance Parameters of DDS

quency Required	W	W Actual	quency Generated	ual Frequency From Simulation
KHz			KHz	KHz
Hz			9 KHz	9 MHz
Hz			Hz	Hz
MHz			KHz	MHz

In this paper, DDFS synthesizer module is deigned in MATLAB based VHDL code and the output is debugged. It is especially designed for FPGA hardware platform. In the simulation various periodical waveform is generated at various frequencies and the results are shown in Figure-5, Figure-5 and in Figure-6. Periodic waveform generation is a major function for all communication

systems. Tuning process is used to control the Synthesization process.

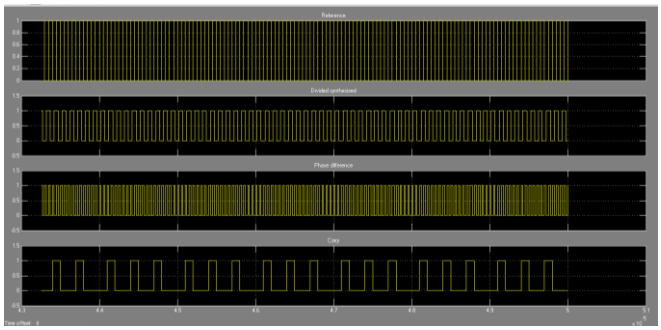

Figure-4: Referencce, Divided Synthesized and Synthesized Signal

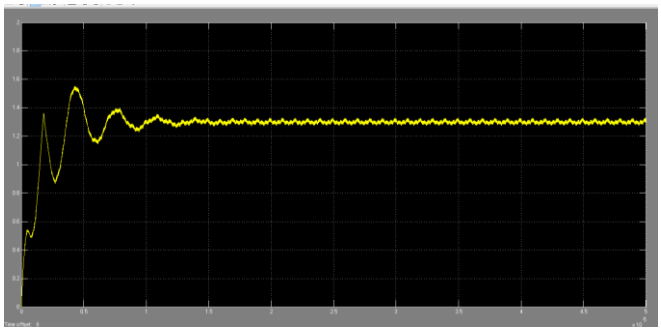

Figure-5: Controled Signal

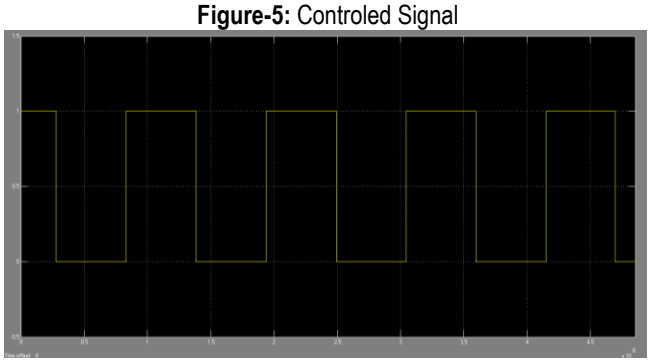

Figure-6: Synthesized Signal

A. Performance Analysis By Comparing with Quantization Based Sine Wave Correction

The periodic wave generation is also generated by quantization method. There are three kinds of quantization process applied are: Phase quantization, Amplitude Quantization and sine wave approximation.

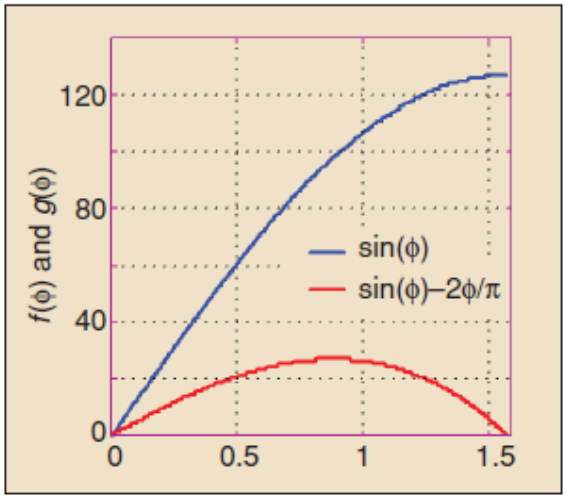

Figure-7: Sine-phase difference LUT example (P= 9, M = 8).

Quantization occurs on both the ACC phase information and on the Output amplitude information. The DDS is now redrawn including this effect. The number of bits used by each variable is written below the variables on Figure 2. In this paper there are two kind of quantization process is applied one is using Phase quantization and the other one is by sine wave approximation. **Phase quantization** occurs when the phase information ACC is truncated from *N* to *P* b as shown in Figure 3. The reason behind this quantization is to keep the memory requirements of the phase to waveform converter quite low: When implemented as a LUT, the size of the memory is 2*P* ×*M* b. A realistic value for *N* is 32, but this would lead to a 232 ×*M* memory that is not realistic. Thus we quantize the phase information _ to *P* b, as it decreases the number of entries of the LUT. The first **sine wave approximation** method goes as follows: instead of storing $f(\Phi) = \sin(\Phi)$ using *M* b, one can store $g(\Phi) = \sin(\Phi) - 2\Phi/\pi$, hence the name *sine-phase difference algorithm* found in [6]. It has been shown in [6] that this new function *g* only needs $M - 2b$ to get the same amplitude quantization for the sine wave (see Figure-7 for an example). The only drawback is the need for an adder at the output of the LUT.

IV. CONCLUSION

In this paper a DDS based output signal correction method is proposed. The proposed approach utilizing quantization methods for synthesizing the output signal. The sine wave approximation method is applied here for

correcting the signals. By getting a best Synthesization by using only a single method cannot provide more accuracy. Hence in this paper we use two different quantization methods for Synthesization in DDS. In Future work the phase locked loop is configured and integrated with DDS for improving the accuracy in terms of frequency Synthesization. Also the performance is evaluated by comparing with the existing quantization process.

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