

MODIFIED BYPASSING MULTIPLIER FOR POWER EFFICIENT FIR FILTER

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Abstract

Low power consumption and smaller area are the most important criteria for the fabrication of DSP systems. Optimizing speed and power of the multiplier is a major design issue. However, speed and power are usual constraints conflicting to each other, so that increasing speed results in larger areas. Parallel multipliers like Braun's multiplier are preferred over serial multipliers as they consume more power. In this paper, we have designed a low power FIR filter, by simplification of addition operation in a bypassing multiplier. The same has been implemented and the power dissipation is calculated. The effectiveness of the proposed technique is also proved by comparing the obtained results with the existing low power FIR filter design.

Keywords – Braun's multiplier, Bypassing multiplier, FIR filter, FPGA.

I. INTRODUCTION

For multiplication of two unsigned n-bit numbers, where the multiplicand is $A = a_{n-1} a_{n-2} \dots a_0$, and the multiplier is $B = b_{n-1} b_{n-2} \dots b_0$. The product, $P = P_{2n-1} P_{2n-2} \dots P_0$, is represented by the following equation:

$$P = P_{2n-1} P_{2n-2} \dots P_0 = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} (a_i b_j) 2^{i+j} \quad (1)$$

In high-performance DSP applications, the parallel array multiplier is widely used and the typical implementation of such an array multiplier is Braun design.

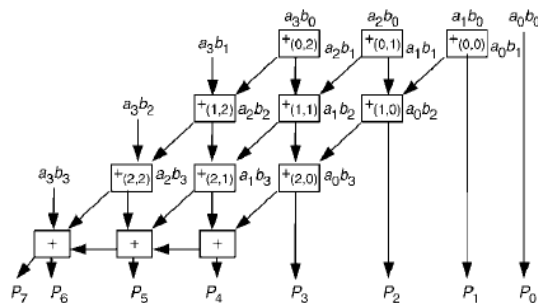


Fig.1: 4X4 Braun multiplier

In a $n \times n$ Braun multiplier[1] the multiplier array consists of $(n-1)$ rows of carry-save adders(CSAs) and a $(n-1)$ -bit ripple-carry adder in the last row, in which each row contains $(n-1)$ full adders(FAs). The $(n-1)$ FAs in the first CSA row that have only two valid inputs can be replaced by $(n-1)$ half adders(HAs).

In CMOS circuits static and dynamic power dissipation are experienced [3]. Static power dissipation is due to the leakage current and the consumption is proportional to the number of transistors used. Dynamic power dissipation is due to the switching transient current and the consumption is obtained from the charging and discharging of the load capacitances. The average dynamic power dissipation for a CMOS gate can be obtained as

$$P_{avg} = \frac{1}{2} C_f V_{DD}^2 \quad (2)$$

Where C =load capacitance, f = clock frequency, V_{DD} = power supply voltage and N = number of switching activities in a clock cycle. If without changing the function the switching activity is reduced, the power consumption can be reduced.

Multiplier unit in DSP applications consumes most of the power [2]. Design of low-power

multipliers in a DSP system is an essential methodology to reduce power dissipation. Many research works have been carried out in the reduction of switching activities[3]. A simple approach for low-power multiplier design is by arranging array of low-power dissipation Full Adders[4]. Other designs like interchanging dynamic operands [5] or using partially guarded computation [6] have also been proposed in the literature. Furthermore, reduced power dissipation can also be achieved through the architectural modification via row bypassing [7] or column bypassing[8] techniques. Based on the concept of row and column bypassing techniques for the reduction of the power dissipation, a low-power 2-dimensional bypassing-based multiplier[9] and a low-power row and column bypassing-based multiplier [10] are further proposed. But still the increase in bypassing circuits decreases the ability of reducing the power dissipation. This necessitates the development of a low power dissipation bypassing multiplier.

In this paper, a low power modified bypassing multiplier is designed by simplification of the addition operations. The same has also been implemented in a FIR filter.

Using our proposed technique modified bypassing multiplier, the various power dissipation factors in a FIR filter were also calculated and a comparison is also made with the existing FIR filter design.

This paper is organized as follows, section II deals with the related works. In section III, the overview of low power bypassing multiplier is discussed. The proposed work is dealt in section IV. The experimental results is discussed in section V. And the paper is concluded in section VI.

II. RELATED WORKS

R. Anitha and V. Bagaveereswaran (2011) designed Braun's Multiplier using Bypassing Techniques. They also implemented the proposed design using Field Programmable Gate Array (FPGA) devices. Wen et al (2005) proposed a low Power Parallel Multiplier design with Column

Bypassing. In this, the authors switched off some columns of the multiplier array whose outputs are known, thus reducing the power dissipation. Sung et al (2008) proposed a Power-Aware 2-Dimensional Bypassing Multiplier. They used Cell-Based Design Flow for increasing the power efficiency.

A proposed Low-Cost, Low-Power Modified Bypassing Multiplier Design reduces switching activity thereby reduces the power consumption.

III. LOW-POWER BYPASSING MULTIPLIER DESIGNS

The general row bypassing adder cell circuit is shown in figure 2. In this, the addition operations in the j th row can be bypassed for the power reduction if the bit, b_j , in the multiplier is 0, i.e., all partial products, $a_i b_j$, $0 \leq i \leq n-1$, are zero. As a result, the addition operations in the j th row of CSAs can be bypassed and the outputs from the $(j-1)$ th row of CSAs can be directly fed to the $(j+1)$ th row of CSAs without affecting the multiplication result. In the multiplier design, each modified FA in the CSA array is attached by three tri-state buffers and two 2-to-1 multiplexers. Because the addition operations of the rightmost FAs in the CSA rows are bypassed, the extra correcting circuits must be added to correct the final multiplication result[7]. Figure 3 illustrates a 4x4 Braun multiplier with row bypassing.

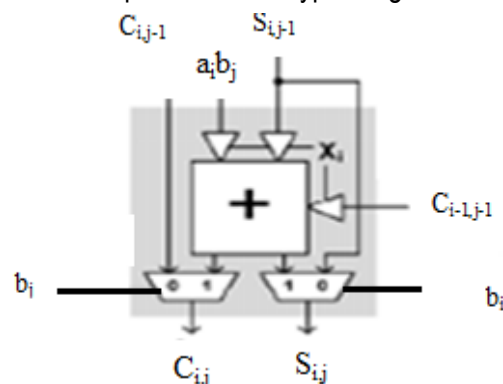


Fig .2: Internal circuit for Row Bypassing Adder cell

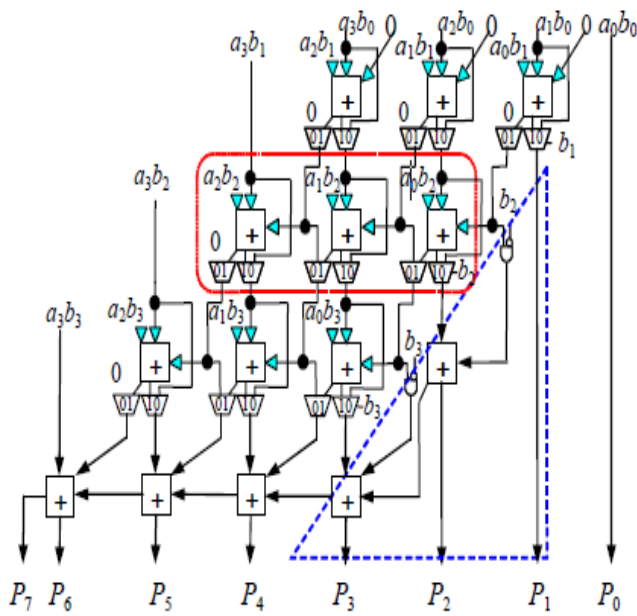


Fig. 3: 4x4 Braun multiplier with row bypassing

Figure 4. illustrates the general column bypassing adder cell circuit. Figure 5. illustrates a 4x4 Braun multiplier with column bypassing. For a low-power column-bypassing multiplier, the addition operations in the $(i+1)^{\text{th}}$ column can be bypassed if the bit, a_i , in the multiplicand is 0, i.e., all partial products, $a_ib_j, 0 \leq j \leq n-1$, are zero.

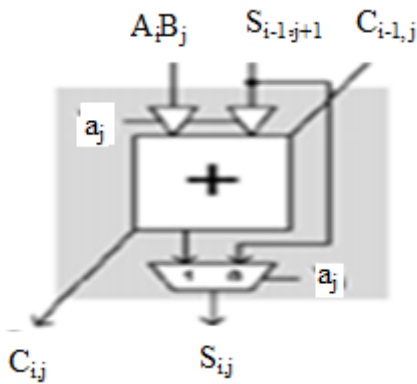


Fig.4: Internal circuit for Column Bypassing Adder cell

In the multiplier design, the modified FA is simpler than that in the row-bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1 multiplexer.

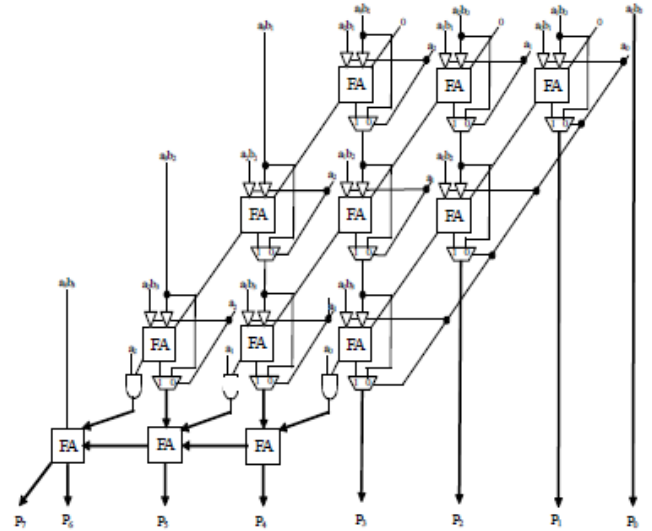


Fig.5: 4x4 Braun multiplier with column bypassing

As the bit, a_i , in the multiplicand is 0, their inputs in the $(i+1)^{\text{th}}$ column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs.

In Fig. 6, a 4x4 Braun multiplier with row and column bypassing can be illustrated. The carry bit in the $(i+1, j)^{\text{th}}$ FA can be replaced by the AND operation of the product, a_ib_j and the carry bit $c_{i,j-1}$.

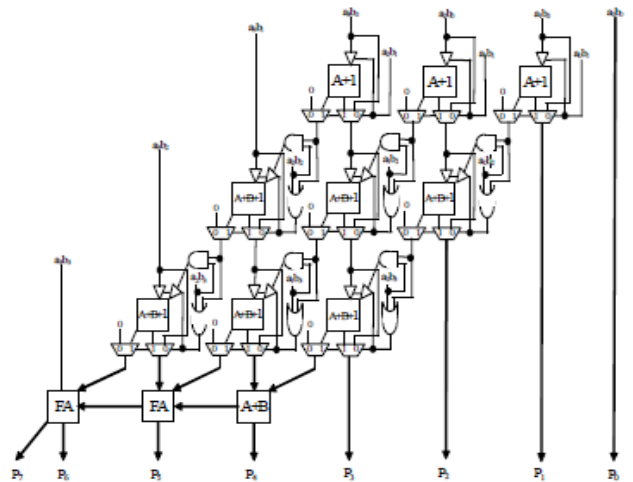


Fig.6: 4x4 Braun multiplier with row and column bypassing

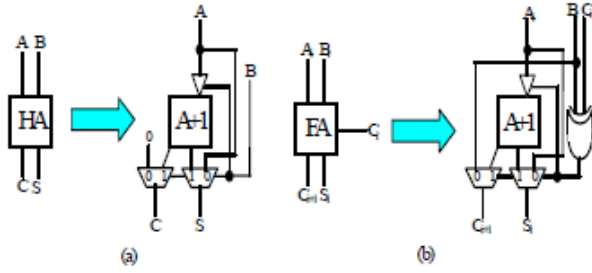


Fig.7: Adders Replaced by Incremental Adder

For the addition operation in FA, the $(i+1, j)^{\text{th}}$ FA, $1 \leq j \leq n$, can be replaced with the modified half adder, $A+B+1$ (Fig.8(c)) and the HAs in the first row of CSAs can be replaced with the incremental adder, $A+1$ (Fig.8(a)). Based on the operation simplification of full adders in an array multiplier, a low-power multiplier with row and column bypassing can be obtained. Besides that, each simplified adder, $A+1$, in the CSA array is only attached by one tri-state buffer and two 2-to-1 multiplexers and each simplified adder, $A+B+1$, in the CSA array is only attached by two tri-state buffers and two 2-to-1 multiplexers.

IV. LOW-POWER MODIFIED BYPASSING MULTIPLIER DESIGN

According to the proposed bypassing condition, it is known that the $(i+1, j)^{\text{th}}$ FA only executes the $A+1$ addition as the product, $a_i b_j$, is not equal to the carry bit, $c_{i,j-1}$. On the other hand, as the product, $a_i b_j$, is equal to the carry bit, $c_{i,j-1}$, the addition result in the $(i+1, j)^{\text{th}}$ FA will be obtained by adding 2 or 0. Therefore, the resultant carry bit, $c_{i+1,j}$, in the $(i+1, j)^{\text{th}}$ FA can be bypassed from the previous carry bit, $c_{i,j-1}$, and the $(i+1, j)^{\text{th}}$ FA can be replaced with a low-cost incremental adder, $A+1$. Besides that, each simplified adder, $A+1$, in the CSA array is only attached by one tri-state buffer and two 2-to-1 multiplexers. Similarly, a HA can be also replaced with a low-cost incremental adder, $A+1$, with the bypassing condition as $a_i b_j = 0$. In Fig. 6, the bypassing-based design of a half adder and a full adder is shown. By using the bypassing-based design of a half adder and a full adder, a 4x4 low-cost bypassing-based multiplier can be illustrated in Fig. 9.

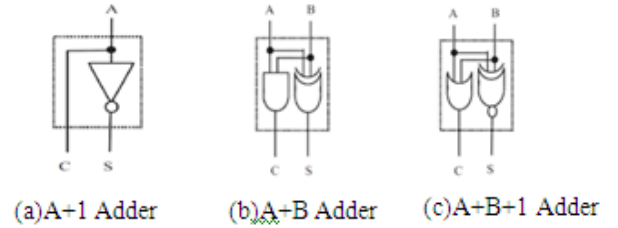


Fig.8: Different Adders in multiplier design

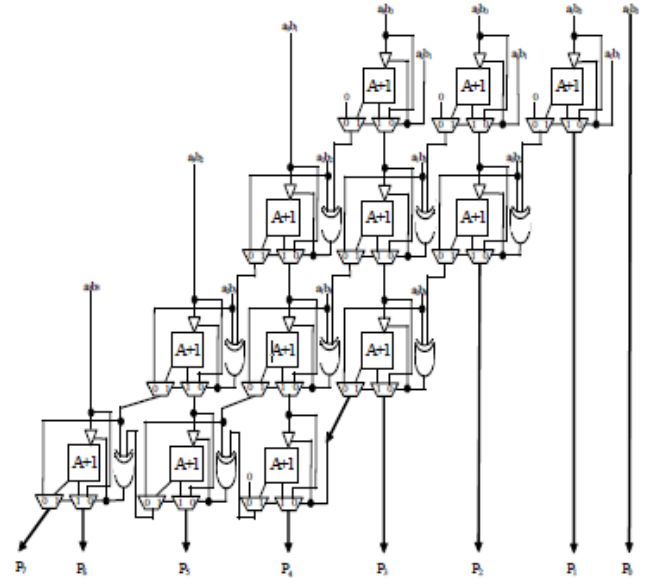


Fig. 9: 4x4 low-cost bypassing-based multiplier

Table 1 shows that the number of transistors used in incremental FA is less than the normal FA. Implementation of Modified bypassing multiplier in a FIR

FILTER

Digital filters can be divided into two categories: finite impulse response (FIR) filters; and infinite impulse response (IIR) filters. Although FIR filters, in general, require higher taps than IIR filters to obtain similar frequency characteristics, FIR filters are widely used because they have linear phase characteristics, guarantee stability and are easy to implement with multipliers, adders and delay elements. The FIR filter chips use memory, an address generation unit, and a modulo unit to access memory in a circular manner. The paper proposes two special features called a data reuse structure and a recurrent-coefficient scheme to provide variable-length taps efficiently. Since the proposed architecture only requires several MUXs,

registers, and a feedback-loop, the number of gates can be reduced over 20 % than existing chips

Table 1: Comparison of Transistor Count

NORMAL ADDER	HALF	INCREMENTAL HALF ADDER (MODIFIED)
Ex-or Gate= 8Trs AND Gate = 6Trs 14Trs	----- -----	2-1 Mux (2) 2x4 =8Trs Tristate buffer =4Trs A+1 Adder =2Trs 14 Trs -----
Need Transistors=14Trs	of	Need Transistors=14Trs
NORMAL FULL ADDER		INCREMENTAL FULL ADDER (MODIFIED)
Ex-or Gate(8x2)=16Trs AND Gate (6x2)=12Trs OR Gate (6x1)=6Trs 34Trs -----		Ex-or Gate(8x1)=8Trs 2-1 MUX =8Trs Tristate buffer =4Trs Incremental adder =2Trs 22Trs -----
Need of Transistor = 34Trs		Need of Transistor = 22Trs

The analysis of linear time-invariant FIR filter is generally carried out by using the Z-transforms. In, general, FIR filtering is described by a simple convolution operation as expressed in the equation

$$Y(n) = \sum_{k=0}^{N-1} h(k).x(n-k) \quad (3)$$

Where $x[n]$, $y[n]$, and $h[n]$ represent data input, filtering output, and a coefficient, respectively and N is the filter order.

FIR FILTER:

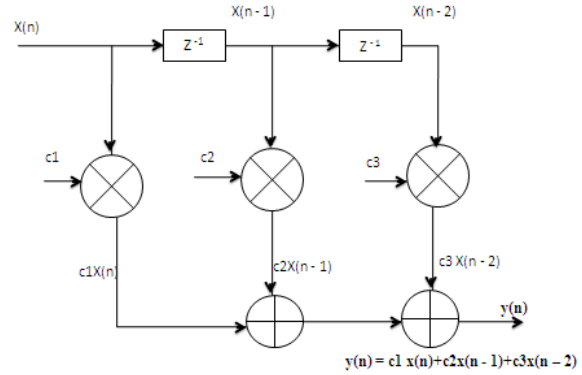


Fig.10: FIR Filter

PROPOSED FIR FILTER:

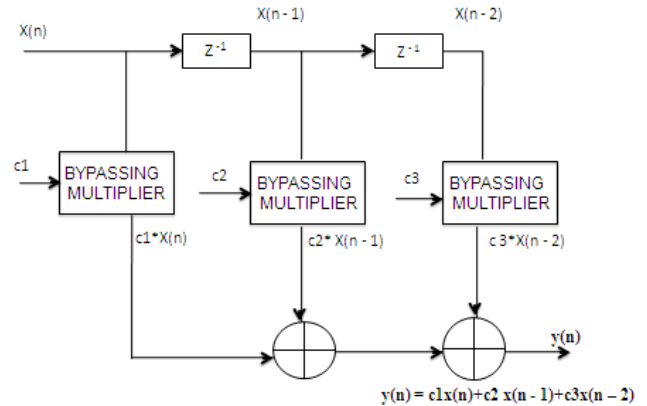


Fig.11: Proposed FIR Filter Design

V.EXPERIMENTAL RESULTS

To implement the FIR filter MODELSIM simulation tool is used. Using QUARTUS II – Altera simulation tool, power dissipation of our proposed design (Modified bypassing multiplier) in a FIR filter and the power dissipation of the existing design in a FIR filter is calculated and compared in table 2.

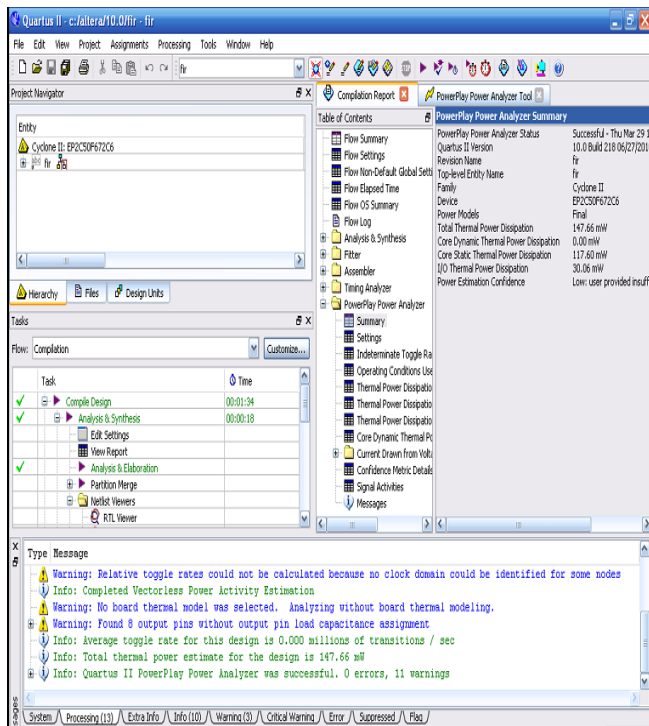


Fig. 12 FIR filter design

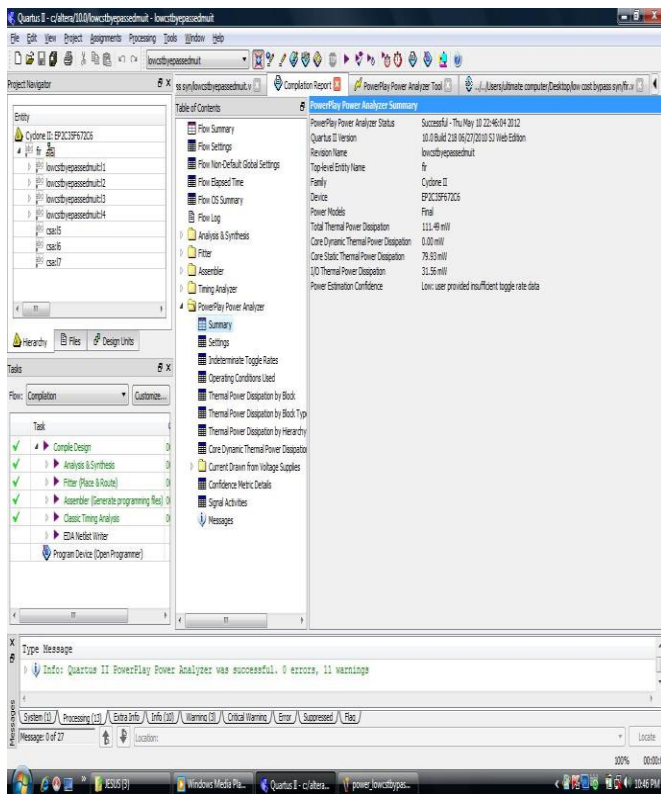


Fig.13 FIR filter design with BYPASSING MULTIPLIERS

Table 2: Comparison of the various power dissipations in a FIR filter.

Parameters	FIR filter design	Proposed FIR filter design
Dynamic Thermal power dissipation	0.00mW	0.00mW
Static Thermal power dissipation	117.60mW	79.93mW
I/O Thermal power dissipation	30.06mW	31.56mW
Total Thermal power dissipation	147.66 mW	111.49 mW

The simulation screenshot of the existing design is shown in figure 12. And the simulation screenshot for the proposed design is shown in figure 13. The comparison on the various power dissipated in a FIR filter using the existing and the proposed technique, we listed in table 2.

VI. CONCLUSION AND FUTURE WORK

In this, we have designed a low power FIR filter using modified bypassing multiplier. The total power dissipation is calculated and compared with the existing technique. The results show that the proposed FIR filter design using modified bypassing multiplier out performs the existing FIR filter design (bypassing multiplier). It is also proved that the proposed technique reduces the power dissipation, reduces the switching activity and achieves high speed.

In future, a low-cost and low-power multiplier can be implemented for 8x8 and 16x16 multiplier design.

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