DESIGN AND ANALYSIS OF N-TYPE CNTFET BASED DOUBLE EDGE TRIGGERED D FLIP-FLOP

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ABSTRACT

This paper enumerates the efficient design and analysis of N-type CNTFET based Double Edge Triggered D Flip-flop. The Flip flop is designed using Ballistic CNTFET (VHDL-AMS model) with the dcnt of 1nm in resistive load inverter logic. The transient and power analysis are obtained with operating voltage at 0.6V for the double edge triggered D flip-flop using system vision tool. There are many issues facing while integrating many number of transistors like short channel effect, power dissipation, scaling of the transistors. To overcome these problems by Considering the carbon nano tube have promising application in the field of electronics. The simulation results are presented, and the power consumptions are compared with the conventional MOSFET design. The comparison of results indicated that the CNTFET based design is capable of efficient power savings.

Keywords: CNT, CNTFET, Resistive load inverter logic, Double edge triggered D flip flop, Circuit simulation.

I. INTRODUCTION

Moore's law describes a long-term trend in the history of computing hardware. The quantity of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years. The trend has continued for more than half a century untill 2007. Recent advancements made this law to continue even after this period.The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors and even the number and size of pixels in digital cameras. All of these are improving at exponential rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy. Moore's law describes a driving force of technological and social change in the late 20th and early 21st centuries[2].

Numerous innovations by a large number of scientists and engineers have became significant factors in the sustenance of Moore?s law since the beginning of the integrated circuit era. Whereas a detailed list of such significant contributions would certainly be desirable, below just a few innovations are listed as examples of breakthroughs that have played a critical role in the advance of IC technology by more than six orders of magnitude in less than five decades. The dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately every two years. This scaling down of devices has been the driving force in technological advances since late 20th century. However further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range[2].

A number of phenomenal advances in CMOS technology by many luminaries in the semiconductor device field since the work of Wan lass have been at the heart of the extremely dense ICs that the industry is able to fabricate today. Within the bounds of MOS technology, the possible circuit realizations may be based on pMOS, nMOS, CMOS and now Bi-CMOS devices, by using these technologies present circuits are designed. As the device dimensions, such as the channel lengths approach to the sub-10 nm regime, direct tunneling between source (S) and drain (D), and severe short channel effects present a fundamental challenge in continued scaling of Silicon devices. As a result, tremendous research efforts have recently been undertaken by various academic and industrial research groups for integrating new semiconductors, as the channel material to enable (i) more efficient transport of carriers that are having higher mobility and (ii) improved electrostatics at nanoscale. In most approaches, a hybrid technology is envisioned, where Si still remains the handling substrate for fabrication processing, heat transport, and mechanical support purposes, with a new semiconductor integrated on the top for enhanced device operations or added new functionalities. One such material system is carbon nano tubes. The unique electron transport properties

and band structure of nano tubes. And by using carbon nano tubes field effect transistor is designed [1, 3].

II. BASICS OF CARBON NANO TUBE STRUCTURES

Carbon nanotubes are discovered in 1991 by S. Ijiima. Carbon nanotubes (CNTs) are hollow cylinders formed by rolling up long chains of carbon atoms in honeycomb structure (Like a ?*chicken mesh*?). This is similar to long tubes with a purely hexagonal structure as shown below. They have attracted much of an attention recently because of their remarkable electronic and mechanical properties[1]. The tube can be a Single Wall Carbon Nanotube (SWNT) or can contain many axial tubes known as the Multi Wall Carbon Nanotube (MWNT). SWNTs are typically one atom in wall thickness, few tens of atoms in circumference and many microns in length and can be either metallic or semi conducting depending on their diameter and chirality. The chirality i.e., the way in which the graphite sheet has been rolled to form a cylindrical structure determines whether the resulting tube is metallic or semi conducting[1,2 and 3].

Fig. 1 shows the carbon nano tube structure. The inner diameter of a MWNT is of the same as SWCNT but the outer diameter may vary from 10nm ~ 100nm depending on the number of co-axial tubes.

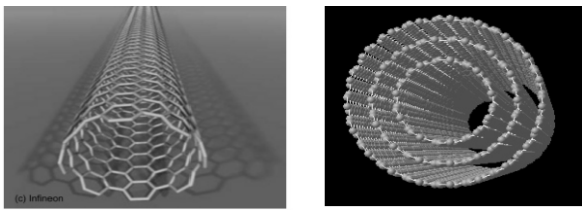

Fig. 1. single and multi walled carbon nano tubes.

III. CARBON NANO TUBE FIELD EFFECT TRANSISTOR

A CNFET is formed by a carbon nanotube connecting two metal electrodes on either side that form source and drain contacts, with gate electrode separated form the nanotube by a thin oxide film. Even though different types of gate structures are in use, a coaxially gated CNTFET is considered for symmetry and optimal results. single-walled carbon nanotube (SWCNT) transistors have attracted intensive attentions for their potential as a novel generation of basic cells in IC design [3]. Fig. 2 shows ballistic CNTFET structure.

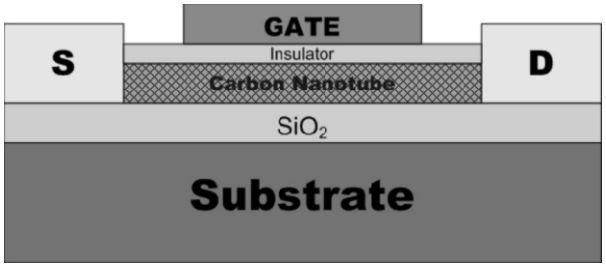

Fig. 2. Ballistic Carbon Nano Tube Field Effect Transistor.

Theoretical and experimental research has demonstrated the unique electrical features of carbon nanotube transistors, including high transconductance and high ON/OFF current ratio. The valence and conduction bands of the carbon nanotube are symmetric, which allows complementary structures in applications. The nearly ballistic transport at low bias implies the possibility of deriving carbon nanotube transistors. Both the metallic and semi conducting nanotubes can be exploited in integrated circuits as interconnection and active devices respectively [3][5][6].

Numerical ballistic CNTFET model

When an electric field is applied between the drain and the source of a CNT, a non-equilibrium mobile charge is generated in the carbon nanotube channel. It can be described as follows[4]:

$$\Delta Q = q\,(N_S + N_D - N_0) \qquad \text{... (1)}$$

Where, N_S is the density positive velocity states filled by the source, N_D is the density of negative velocity states filled by the drain and N_0 is the equilibrium electron density. These densities are determined by the Fermi-Dirac probability distribution:

$$N_S = 1/2 \int_{-\infty}^{\infty} D(E)\, f(E - U_{SF})\, dE \qquad \text{... (2)}$$

$$N_D = 1/2 \int_{-\infty}^{\infty} D(E)\, f(E - U_{DF})\, dE \qquad \text{... (3)}$$

$$N_0 = \int_{-\infty}^{\infty} D(E)\, f(E - E_F)\, dE \qquad \text{... (4)}$$

Where, $D(E)$ is the density of states, f is the Fermi probability distribution, E represents the energy levels

per nanotube unit length, and U_{SF} and U_{DF} are defined as

$$U_{SF} = E_F - qV_{SC} \quad \text{... (5)}$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS} \quad \text{... (6)}$$

Where, E_F is the Fermi level, q is the electronic charge and V_{SC} represents the self-consistent voltage whose presence in these equations illustrates that the CNT energy band is affected by external terminal voltages. The self-consistent voltage V_{SC} is determined by the device terminal voltages and charges at terminal capacitances by the following non-linear

algebraic equation [4]:

$$V_{SC} = \frac{Q_t - q\,N_s\,V_{SC} = qN_D\left(V_{SC}\right) = qN_c}{C\Sigma} \quad \text{... (7)}$$

Where, Q_t represents the charge stored in terminal capacitances and is defined as

$$Q_t = V_G\,C_G + V_D\,C_D + V_S\,C_S \quad \text{... (8)}$$

Where, C_G, C_D, C_S are the gate, drain, and source capacitances respectively.

And the total terminal capacitance $C_{\dot{O}}$ can be derived by

$$C_\Sigma = C_G + C_D + C_S \quad \text{... (9)}$$

According to the ballistic CNT transport theory [1], [10] the drain current caused by the transport of the non-equilibrium charge across the nanotube can be calculated using the Fermi-Dirac statistics as follows:

$$IDS = \frac{2\,qKT}{\pi\,k}\left[F_D\left(U_{SF}/kT\right) = F_0\left(U_{DE}/kT\right)\right] \cdots \quad (10)$$

Where, F_0 represents the Fermi-Dirac integral of order 0, k is Boltzmann's constant, T is the temperature and h is reduced Planck's constant. Since the self-consistent voltage V_{SC} is directly obtained from the spline model, the evaluation of the drain current poses no numerical difficulty as energy levels U_{SF}, U_{DF} can be found quickly from equations 5,6 and I_{DS} can be calculated using:

$$I_{DS} = \frac{2\,qKT}{\pi\,k}\left[\log\left(1 + e^{\frac{E_1 - q\,V_{5c} - V_{D5}}{kT}}\right)\right. \quad \text{... (11)}$$

IV. RESISTIVE LOAD INVERTER LOGIC

As a first step towards competitive logic gate performance, several research groups have proven that CNTFETs can be used to construct various electronic functions, such as logic gates. The first logic circuits with field-effect transistors based on single carbon nanotubes were built as resistive-load circuits[5]. Local gates provided good capacitive coupling between the gate and nanotube, thus enabling strong electrostatic doping of the nanotube from *p*-doping to *n*-doping, as well as integration of multiple devices on a single chip[5]. The inverter circuit is shown in fig.3 was demonstrated to exhibit a range of digital logic operations with supply voltage was 0.6V.

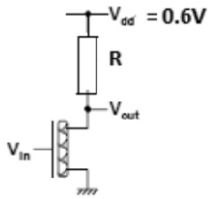

Fig. 3.CNTFET based Resistive load logic circuit

V. DOUBLE EDGE TRIGGERED D FLIP-FLOP

Latch is the basic unit for composing a flip-flop. The levels of a clock, *CLK*, are used to drive the latch to either the storage state or the input state. If we use *D*, *Q* and *Q'* to express the input signal, present state and next state of a latch, the state equations for positive and negative level-sensitive latch can be expressed as:

$$Q' = D \cdot CLK + Q \cdot CLK \quad \text{... (12)}$$

$$Q' = D \cdot CLK + Q \cdot CLK \quad \text{... (13)}$$

Equation (12) describes a latch which passes the input data when *CLK*= 1 and stores it when *CLK* = 0. Inversely, equation (13) describes a complementary latch, which receives input data at *CLK* = 0 and stores it at *CLK* = 1. The corresponding logic structures can be realized with a MUX, as shown in Fig.4.

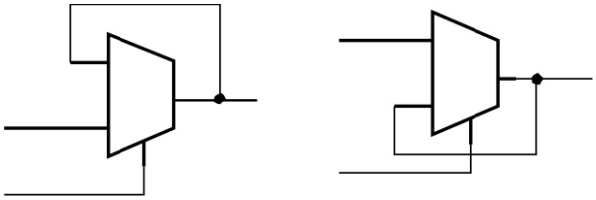

Fig. 4. Positive and negative level-sensitive latches

In single edge triggered D flip flop, whenever there is a rising edge of clock occurs then the output state will be changed. A Double edge- triggered (DET) D- flip-flop, [7] which samples the input data by both the clock rising edge and falling edge. If the input data has to be received at both clock levels, the two complementary latches should be connected in parallel. Then we can obtain a side-by-side flip-flop as shown in Fig.5 Since the flip-flop is required to be non transparent from input to output, the output terminal should always be connected to the latch which is in storage state. Therefore, the MUX framed by the dotted line is needed. Because the flip-flop's state can change at both falling and rising edges of the clock[7]. The Double Edge Triggered D Flip-flop internal diagram is shown in fig 5.

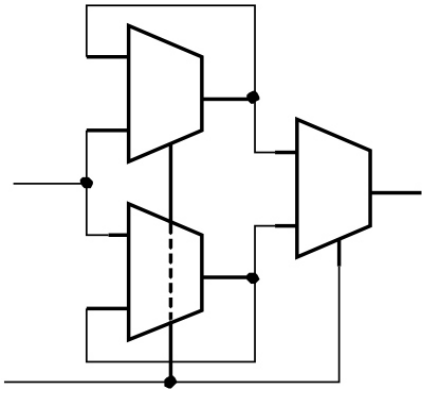

Fig. 5. Double Edge Triggered D Flip flop

This paper investigates the principles of the DET flip-flop design in resistive load inverter logic with N-CNTFET, and presents a logic structure based on multiplexors. This design can also be used for reducing power dissipation while preserving the data through put or doubles the data throughput while preserving the power dissipation.

VI. TRANSIENT ANALYSIS

The N-type CNTFET, Resistive load CNTFET Inverter, Multiplexer and the Double edge triggered D Flip flop are simulated at 0.6Volt using system vision tool. The Ids Vs Vds Characteristics of the CNTFET is shown in the Fig.6.

The transient analysis of the CNTFET based resistive load inverter is shown in the Fig.7.

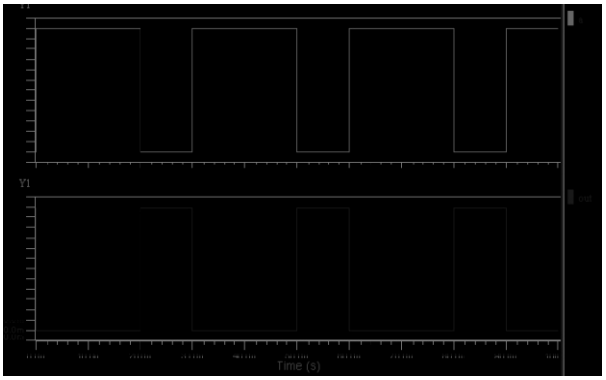

Fig. 7 Simulation of Resistive load N-type CNTFET Inverter

The transient analysis of the CNTFET based 2X1 Multiplexer is shown in the Fig.8.

The transient analysis of the CNTFET based Double edge triggered D Flip- Flop is shown in the Fig.9.

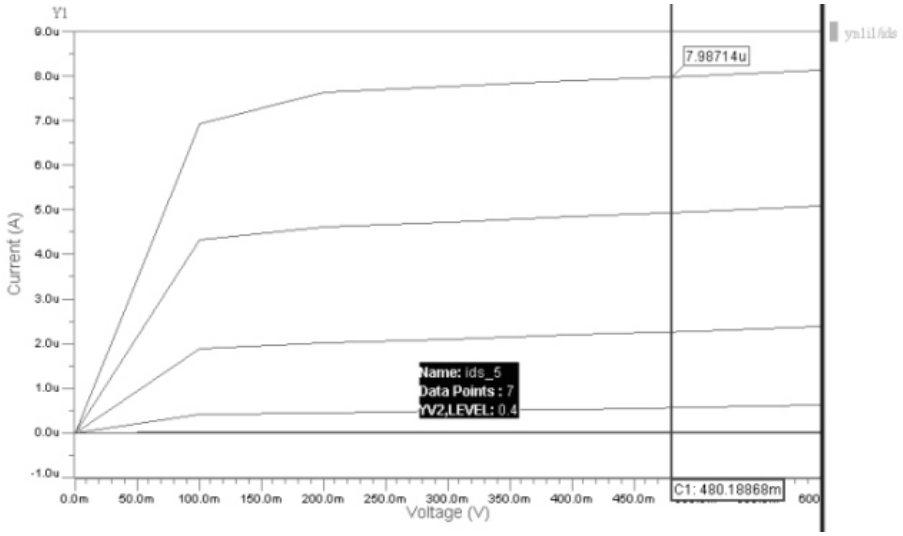

Fig. 6 Ids vs Vds characteristics of CNTFET

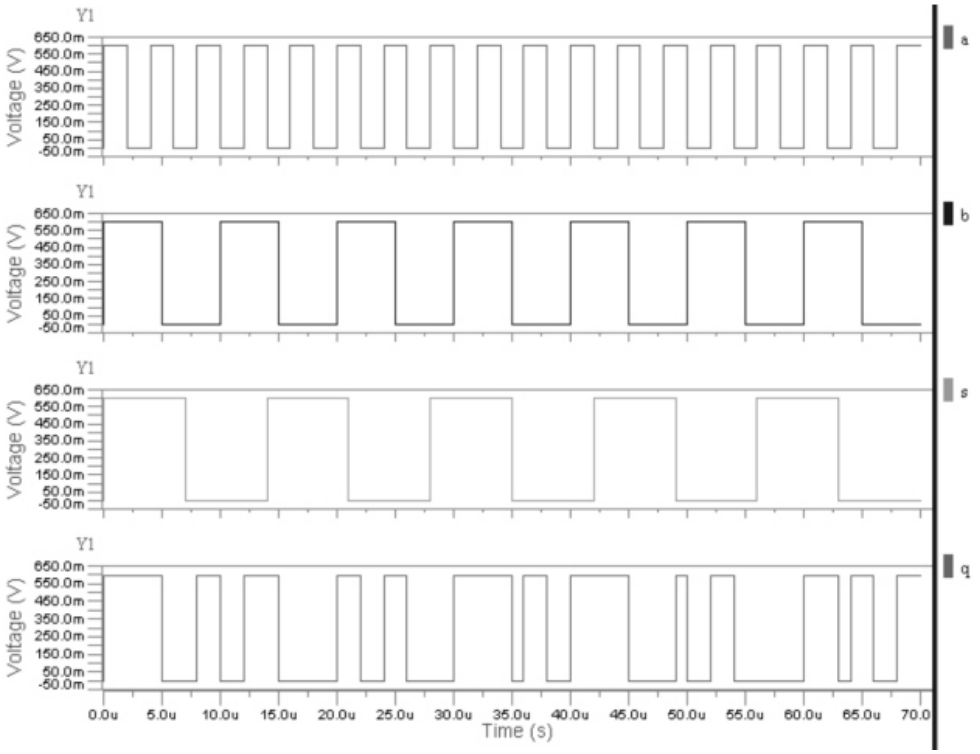

Fig. 8 Simulation result of 2X1 Multiplexer

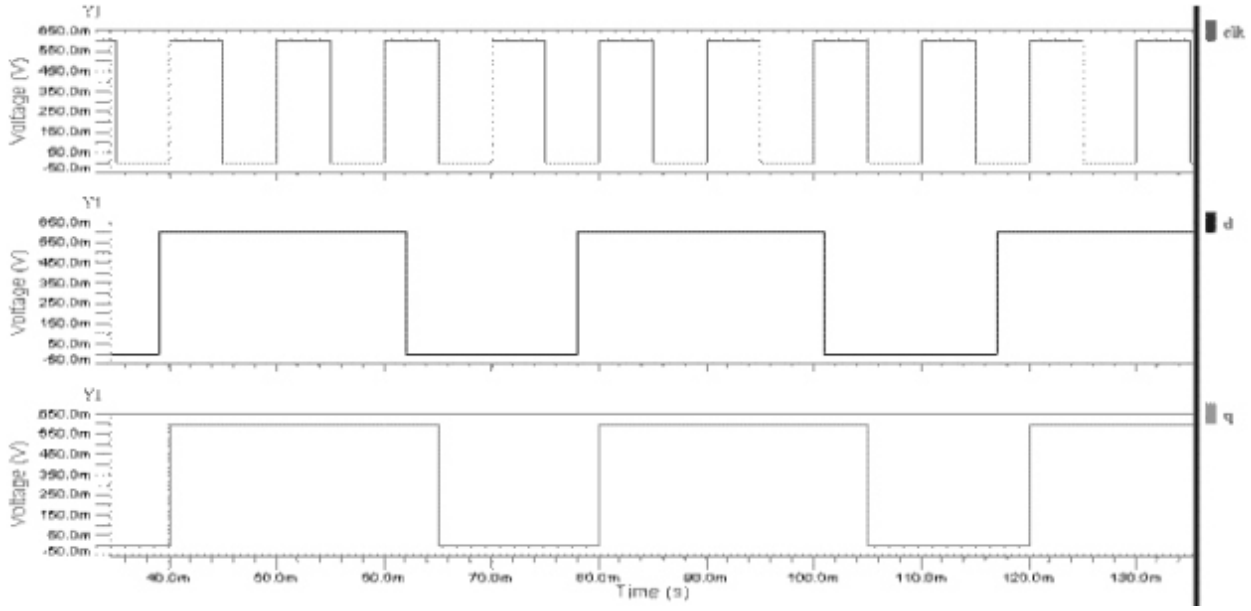

Fig. 9. Simulation result of Double Edge Triggered D Flip-Flop

VII. POWER ANALYSIS

The Double edge triggered D flip flop power analysis were done and the power consumption of CNTFET based design has been compared with the MOSFET based design. Table-1 and Fig.10 shows power analysis of the Double Edge Triggered D Flip-flop.

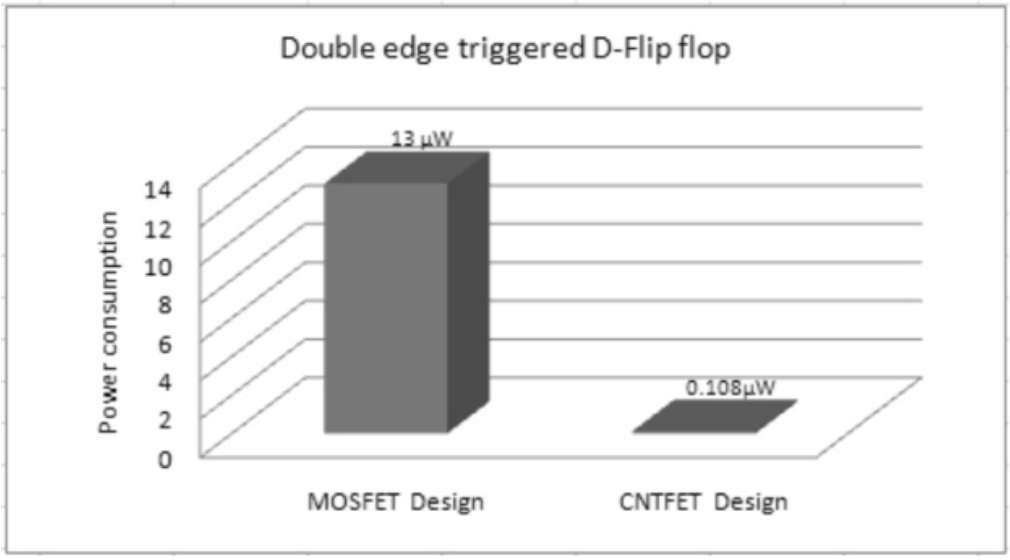

Fig. 10 Power Analysis Of Double Edge Triggering D Flip-Flop

Table 1. Power Analysis of Double Edge Triggered D Flip-Flop

D flip-flop	MOSFET (conventional)	CNTFET (dcnt = 1nm)
Double Edge Triggered D flip-flop	13uW	0.108uW

VIII. CONCLUSION

The inverter, 2X1 multiplexer and the Dougble Edge Triggered D -Flip flop is designed using Ballistic CNTFET with the diameter of CNT as 1Nano meter in resistive load inverter logic. The transient analysis were obtained for inverter, Mux and Double edge triggered D flip-flop and the power analysis were obtained for the Double edge triggered D flip-flop. The designs are simulated with operating voltage of 0.6V using system vision tool. The power consumption results of CNTFET based Design are compared with the conventional MOSFET Design. The CNTFET based design of Double edge triggered D-flip flop is more better power efficient than MOSFET design.

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