DIGITAL DOWN CONVERTER IMPLEMENTATION OF ASIC USING IN IP

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ABSTRACT

Multirate systems are the systems that function at multiple sample periods. One example of such a system is a Digital Down Converter, used in digital communication receivers. Digital down conversion is a basic process of any digital communication receiver, where the bandwidth of the beloved channel centered at carrier frequency, is shifted down to baseband signal centered at zero frequency. Any digital communication receiver will have an Analog to Digital Converter, sampling and digitizing the selected channel at tens or hundreds of MHz, thus producing a very high data rate. It is outside the real time computational capabilities of the slower software processors to further process this signal at such a high rate. The DDC is placed in between the fast ADC and the slower signal processors, in a digital communication receiver. The DDC basically performs two functions. It first downconverts the bandwidth of the selected channel to baseband i.e. centered at zero frequency, and then it reduces the sample rate or downsamples the signal to a lower rate. By doing so, it becomes easier for the following stages, which consists of lower speed processors to further process the signal. DDC's are most usually implemented in logic using Field Programmable Gate Arrays or Application Specific Integrated Circuits. In the course of this project, one such DDC is implemented in ASIC, which can be later used as an Intellectual Property.

KEY WORDS *:* Digital down conversion, Digital Converter, sampling, ADC,etc.

I. INTRODUCTION

An essential component of any digital communication receiver is the Digital Down Converter. Development in the field of Digital Signal Processing has helped DDC to become a basic component of any digital communication receiver. The job of the DDC is to take a digital signal either band limited or centered at an in-between frequency and shift it down to baseband, centered at zero frequency. The DDC also filters noise and unnecessary components in the process.

Thus there arises a need for the DDC, which has to somehow reduce the rate of the sampled signal, allowing further easy signal processing by smaller speed processors. The DDC achieves this by doing two effects,

i. First, the DDC shifts the bandwidth of the selected channel which is centered at carrier frequency to a baseband signal centered at zero frequency.

ii. The DDC then downsamples or reduces the number of samples of this baseband signal which is centered at zero frequency.

The DDC block belongs to a class of systems recognized as multi rate systems. These systems operate at multiple sampling rates. It is used extensively in wireless and wired communication receivers. Some typical applications that use DDC are,

i. Software Defined Radios.

ii. Digital Receivers.

iii. Cable Modems.

iv. Quadrature Amplitude Modulation Modems.

v. CDMA 2000 and 3G Base Stations.

II. SUMMARY OF DDC'S FUNCTIONALITY

An summary of DDC's functionality is shown in Figure 1.1. As an example, consider a digital communication receiver such when a Software Defined Radio. Let the SDR select a channel deceitful in the range of 39-40 MHz. The signal bandwidth is thus 1MHz centered on a carrier frequency of 39.5 MHz. This channel is selected using a filter, which is usually built using analog method. However, the ADC takes the selected channel as input, and digitizes the selected channel with a sampling frequency of 200 MHz. The output data rate of the ADC thus becomes 200 MB/s.

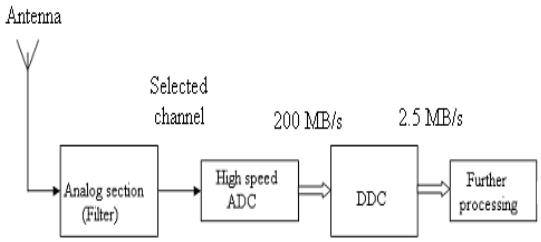

Fig1. An overview of the DDC's functionality.

Now, the DDC first shifts or down converts the selected channel's bandwidth, centered at 39.5 MHz, down to baseband centered at zero frequency. This is done by multiplying or addition the output of the ADC with a digital sine/cosine wave whose frequency is equal to that of the carrier frequency of the selected channel. This sine wave is generated by a digital local oscillator, which is also called as Direct Digital Synthesizer in DSP systems. The DDS is a sub block of DDC.

The result of multiplying the chosen channel with a sine wave generated by DDS is shown in Figure. Here, the process generates two signals, the baseband signal and the one centered at $2f_c$, where f_c is the carrier frequency. The baseband signal is then selected using suitable filter.

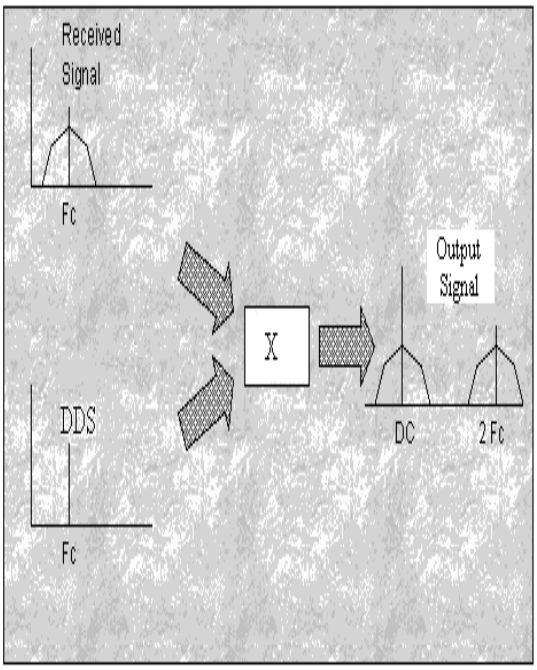

Fig.2 Shifting the bandwidth of the selected channel.

Once the selected signal is down converted, the sampling rate can now be reduced. With a channel of 1 MHz bandwidth centered at zero frequency, a sampling rate of 2.5 MHz would be enough, giving a data rate of only 2.5 MB/s. Therefore the DDC now downsamples the output of ADC from 200 MB/s to 2.5 MB/s. Thus it becomes easier for the scheduled low speed software processors to process the output of the DDC, which is a signal of data rate 2.5 MB/S.

As regards the Project

The check setup of DDC implemented in this project is shown in Figure The input to the DDS is a clock signal of frequency 100 MHz. The DDS takes this clock signal as input and generates a sine wave signal. The baseband signal generated by the DDS is a sine wave signal of 1.5 MHz. The output of the DDS is directly fed to the CIC filter.

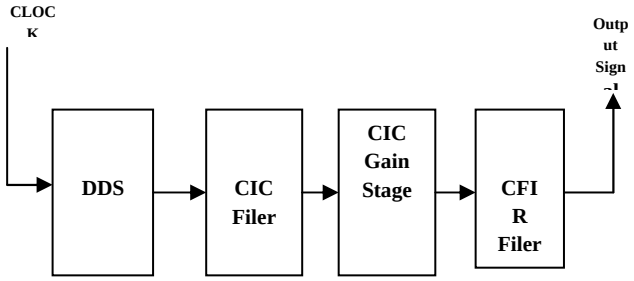

Fig3: Test setup of DDC block diagram.

Problem Classification

High frequency signal in the range of 30MHz to 100MHz is need to be down converted to baseband signal whose frequency is 1.5MHz. The incoming signal which has information in the amplitude is very responsive to noise. Hence, there is a need for high speed, highly accurate DDC which can down convert and also downsample the incoming signal by a factor of 16. The DDC should be reconfigurable to be designed and implemented using ASIC technology.

Problem Statement

To design and implement a DDC chip, using Application Specific Integrated Circuit technology.

Project Objective

i. To design the DDC block, where the input signal occurrence is 1.5 MHz.

ii. The input signal should be downsampled by a factor of 16.

iii. To target the hardware on ASIC of 1.3 nm technology.

iv. The chip, after designing, should consume minimum amount of power during operation.

Attitude Adopted to Meet the Objectives

i. Collecting in sequence concerning the functionality of the various sub blocks of the DDC block.

ii. Scheming of the sub blocks to gather the project specifications.

iii. Mounting Hardware Description Language, such as Verilog, for the various sub blocks using Modelsim tool.

iv. Efficient simulation of the Verilog code for the sub blocks using Modelsim tool.

v. Synthesis of the Register Transfer Level code using Design Compiler tool from Synopsys.

vi. Implementing physical design of the DDC using Astro tool from Synopsys.

III. DDC ARCHITECTURE – IMPLEMENTATION AND SIMULATION

The primary step in scheming the DDC chip is to develop a Hardware Description Language code for the DDC. The RTL code is developed at a behavioral level using appropriate HDL. The HDL used in this project is Verilog. This chapter first gives a explanation or the behavior of the sub blocks of DDC, which serves as a root to develop the HDL code. This chapter also explains how the Verilog code for sub blocks of DDC is implemented using a suitable flowchart. The efficient simulation and the results of simulation are also discussed. The design begins with the modular approach of sub blocks.

DDS Block

The DDS block is developed using a LUT of 63 ten bit sine values. The bit width used for the sine wave is 10bits. Frequency of the sine wave generated is about 1.5 MHz for a 100 MHz clock. The number of samples used to generate one single cycle of wave is 63.

The output of the DDS block simulated in Modelsim is shown in Figure. To see the wave in analog form, the signal is formatted using analog step method. The pixel values entered are -200 and 0.3. In Figure the top wave is the clock which is compressed in the time scale due to its high frequency, and the lower wave is the sine wave.

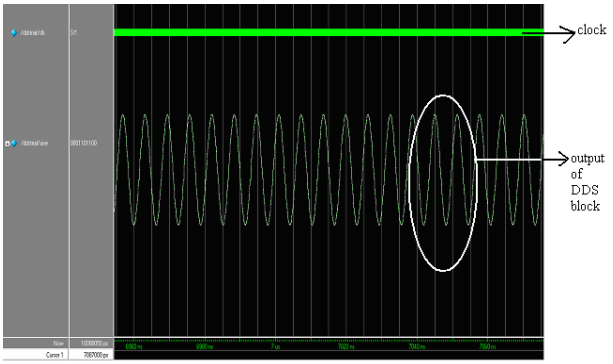

Fig.4: Output of the DDS block in Modelsim.

Output of the Booth's Multiplier

Booth's multiplier is simulated by performing multiplication of two 8 bit operands. The output of the Booth's multiplier simulated in Modelsim is shown in Figure. During simulation, multiplication is performed taking different values for operands 'a' and 'b'.

The multiplier has an enable signal 'en' when asserted to 1 gives the product in one clock cycle. When both the operands are positive the product is a positive product. If any one of the operands changes sign, the product becomes negative indicating signed multiplication. The case where both the operands are negative giving a positive value for the product further proves the concept that the multiplier is a signed multiplier.

From Figure it can be seen that, the results for the multiplier are validated for operands in 2's complement notation. The values given were, a=15, b=15, and the result obtained was, c=225.

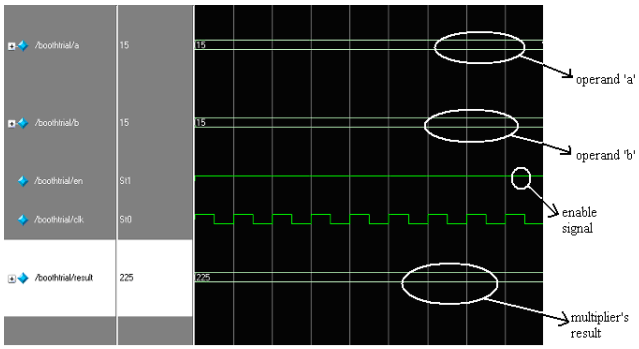

Fig:5 Output of the Booth's multiplier in Modelsim.

Output of the CIC Filter

The output of the CIC filter block simulated in Modelsim is shown in Figure. To see the wave in analog form, the signal is formatted using analog step method. The pixel values entered are -2500 and 0.025. The top wave is the sine wave generated by DDS. This sine wave is fed as input to the CIC filter. The lower wave is the output of the CIC filter. The input given to the filter is a scaled sine wave of 63 samples of width 10 bits. The input samples are passed through two integrators and two differentiators of the CIC filter. Gain of the sine wave is restricted by adjusting the accumulator bit width. Output from the block is as expected, a recovered sine wave but downsampled by a factor of 8.

The results of the CIC filter can be seen in Figure for a 100 MHz clock period.

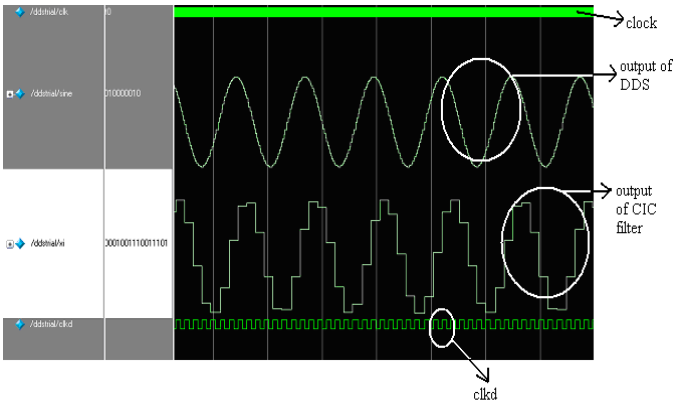

Fig:6 Output of the CIC filter in Modelsim.

Output of the CFIR Filter

The output of the CFIR filter block simulated in Modelsim is shown in Figure. To see the signal in analog form, the signal is formatted using analog step method. The pixel values entered are -30500 and 0.0025.

The top wave is the output of CIC filter represented as xi. The signal xi is fed as input to the CFIR filter. The lower wave is the output of the CFIR filter, represented as yq.

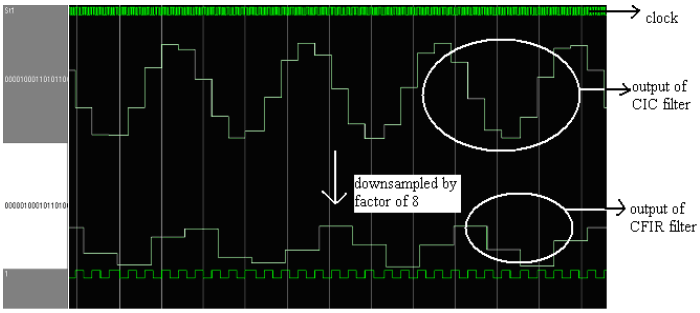

Fig:7 Output of the CFIR filter in Modelsim.

From Figure it can be seen that the output of the CFIR filter is the same sine wave, but downsampled further by a factor of 2, or "xi" is downsampled from 8samples to 4 samples. Scaling of the output wave is done, to accommodate the entire wave. Apart from downsampling the input signal, the CFIR filter also compensates for the drop in the gain of the signal. This is manifest from the CFIR filter output shown in Figure. Without the CFIR filter, the amplitude of the resultant output signal would be very small.

Final output of the DDC

The final output of the entire DDC on a single screen is shown in Figure. The top wave is the output of the DDS, the middle wave is the output of the CIC filter block, and the lower wave is the output of the CFIR filter block. The output of CFIR filter block is the final output of the DDC.

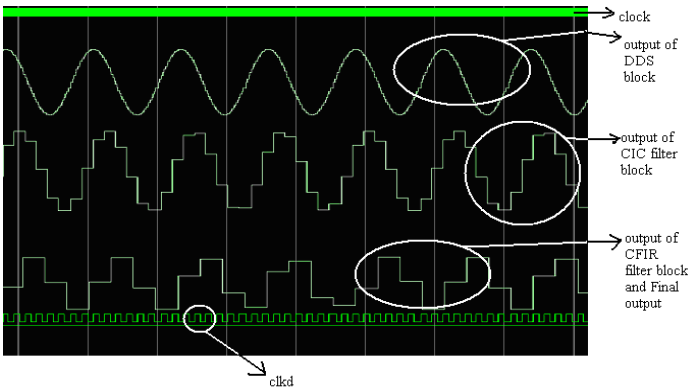

Fig:8 Final output of the DDC.

Outputs of the DDC block are 18-bit samples that can be processed by a conventional DSP processor. The results of the functional simulation clarify that the Verilog code for the DDS, CIC filter, CFIR filter and Booth's multiplier are functionality wise correct. These codes are then given as input to the logic synthesis tool for synthesis.

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