FPGA PROTOTYPING OF CONFIGURABLE SAMPLING RATE CONVERTER FOR SOFTWARE DEFINED RADIO (CSR-SDR) USING CIC FILTER

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Abstract

A Software Defined Radio (SDR) system is a radio communication system, which uses software for modulation and demodulation of radio signals. In software defined radio (SDR) receivers, high-precision clock with very low jitter is required. It is intuitive to use only one fixed master clock. However, different wireless standards use different master clock rates. Under such circumstances, digital sample rate conversion (SRC) can be used as an important solution to provide different clock rates. The basic methods used in the SRC technology are decimation with down-sampling and interpolation with up-sampling, Down-sampling has to be preceded by filtering in order to avoid aliasing, while up-sampling must be followed by filtering to reject spectral images. In this paper, the design was implemented in FPGA using Verilog. The sampling rate conversion is performed by sampling the incoming signal and interpolating/decimating the signal to the desired value and then applying the low pass filter to eliminate aliasing. The sampling is done by digital mixer (Numerical controlled oscillator). The Interpolation/Decimation is performed by the CIC filter. FIR filter performs the low-pass filtering. The sampling rate converted value is given to the DSP processor for further processing. The projected application of the CSR_SDR are in GSM handset, CDMA handset and all the wireless applications. In this paper the functionality has been implemented, verified and checked using Verilog.

Key words: Software Defined Radio, FPGA, Interpolator, Decimator etc .

I. INTRODUCTION

Normally, the implementation of filter would be done as an algorithm developed in the processor in case of the digital receiver/transmitter section. It would be an analog circuitry if it would be an analog receiver/transmitter section. When the filter design is implemented with the analog circuitry, it would occupy more power, space and it would not be configurable. Again, if we have implemented with the DSP processor the filter can be made configurable but dynamism would be missing and also it would be pity slow for higher frequencies. In high frequency application, a separate processor would be needed to implement the filter, this would increase the cost of the application. In the case of Mixer circuit, it is normally implemented by using analog circuitry, whose performance deviates as time passes and it degrade the performance.

ASIC requires very low power consumption, area and it provides functional specific application. The per chip price also would be very less for an application. ASIC could be configured by the processor that is running in the application. It is very much suitable for bulk production of products. It is also to eliminate the processing power of the processor, as the ASIC going to perform all the required functionalities and processor is going to handle only the higher layer implementation. ASIC development would be proceeded by FPGA prototyping.

The proliferation of wireless standards—including wide area 3G, 2.5G, and local area 802.11 networks—future wireless devices will need to support multiple air-interfaces and modulation formats. Software defined radio (SDR) technology enables such functionality in wireless devices by using a reconfigurable hardware platform across multiple standards. With FPGA and data converter technology continuously evolving, SDR concept is increasingly becoming a reality.

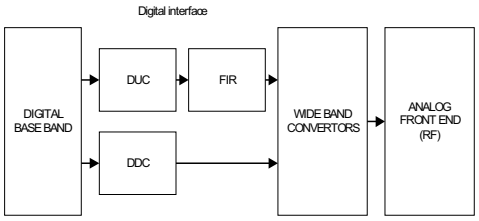

Fig.1. Reconfigurable Hardware Architecture of Software Defined Radio

Fig.1 illustrates the hardware architecture of an SDR that can be reconfigured to support multiple standards. In which digital baseband corresponds to a DSP signal processor which does all the high level signal processing applications. In order to reconfigure the entire system, an ideal SDR base station would perform all signal processing tasks in the digital domain. However, current-generation wideband data converters cannot support the processing

bandwidth and dynamic range required across different wireless standards. As a result, the analog-to-digital converter (ADC) and the digital-to-analog converter (DAC) are usually operated at intermediate frequency (IF) and separate wideband analog front ends are used for subsequent signal processing to the radio frequency (RF) stages.

Digital IF extends the scope of digital signal processing beyond the baseband domain out to the antenna—to the RF domain. This increases the flexibility of the system while reducing manufacturing costs. Moreover, digital frequency conversion provides greater flexibility and higher performance (in terms of attenuation and selectivity) than traditional analog techniques. FPGA implementation provides a flexible and integrated platform to implement computationally intensive digital IF functions including digital up-down converters.

The Digital section consists of

I) Digital Up-converter.

ii) Digital Down converter.

iii) FIR Filter.

B. Digital Up Converter

Generally, the Digital Up Converter is a digital circuit which implements the conversion of a complex digital baseband signal to a real pass band signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The DUC typically performs pulse shaping and modulation of an intermediate carrier frequency appropriate for driving a final analog up converter and is used extensively in wireless and wire line communication systems

Data formatting is required between the baseband processing elements and the up converter can be seamlessly added at the front end. This technique provides a fully customizable front end to the up converter and allows for channelization of high-bandwidth input data, which is found in many systems. Custom logic or embedded processor can be used to control the interface between the up converter and the baseband processing element.

A DUC is a digital circuit which converts a digital baseband signal to a pass band signal. The input baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The baseband signal is filtered and converted to a higher sampling rate before modulating a direct digitally synthesized (DDS) carrier frequency. The input signals are passed through three filtering stages. Each stage first filters the signals with a low pass interpolating filter and then performs a sampling rate

The DUC is made up of CIC filter and FIR filter. The coefficients of both the filter can be varied on based on the requirement. The filters are implemented in fixed-point mode. The input/output word length and fraction length are specified. The internal settings of the first two filters are specified, while the internal settings of the CIC filter are calculated automatically to preserve full precision.

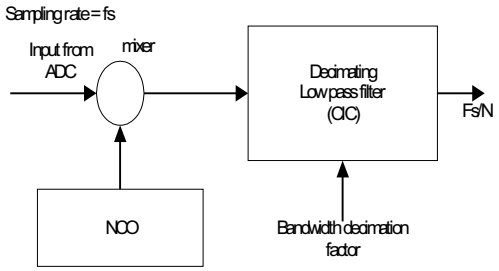

Fig.2 Digital Up Converter

Fig-2, shows the operation of the digital up converter. It consists of numerically controlled oscillator (NCO) and interpolating low-pass CIC filter. In digital up conversion, the input data is baseband filtered and interpolated before it is send to the RF.

C. Digital Down Converter

On the receiver side, digital IF techniques can be used to sample an IF signal and perform channelization and sample rate conversion in the digital domain. Digital Down-Converters (DDC) is a key component of digital radios. The DDC performs the frequency translation necessary to convert the high input sample rates found in a digital radio, down to lower sample rates for further and easier processing.

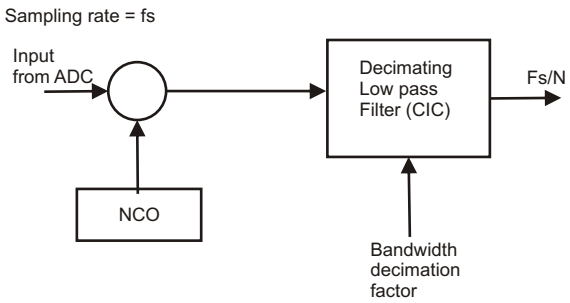

Fig. 3 Digital Down converter

The DDC is made up of CIC filter and FIR filter. The coefficients of the both the filter can be varied, based on the requirement. The filters are implemented in fixed-point mode. The input/output word length and fraction length are specified. The internal settings of the first two filters are

specified, while the internal settings of the CIC filter are calculated automatically to preserve full precision. The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to quadrature down convert the input signal to baseband. The baseband signal is then low pass filtered by a Cascaded Integrator-Comb (CIC) filter followed by two FIR decimating filters to achieve a low sample-rate.

The final stage often includes a resampler which interpolates or decimates the signal to achieve the desired sample rate depending on the application. Further filtering can also be achieved with the resample. A block diagram of a typical DDC is shown in the fig.3.

D. CIC Filter

Cascaded integrator-comb (CIC) digital filters are computationally efficient implementations of narrowband low pass filters and are often embedded in hardware implementations of decimation and interpolation in modern communications systems. CIC filters were introduced to the signal-processing community, by Eugene Hogenauer, more than two decades ago, but their application possibilities have grown in recent years.

Improvements in chip technology, the increased use of polyphase filtering techniques, advances in delta-sigma converter implementations, and the significant growth in wireless communications have all spurred much interest in CIC filters.

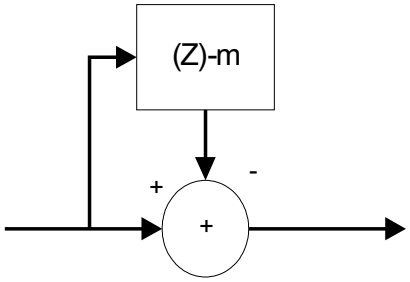

Fig. 4 Feed forward comb structure

CIC filters are well-suited for antialiasing filtering prior to decimation (sample-rate reduction), and for anti-imaging filtering for interpolated signals (sample-rate increase). Both applications are associated with very high—data-rate filtering, such as hardware quadrature modulation and demodulation in modern wireless systems and delta-sigma A/D and D/A converters.

Because their frequency-magnitude-response envelopes are sin(*x*)/*x*-like, CIC filters are typically either followed or preceeded by higher performance linear-phase low pass tapped-delay-line FIR filters whose tasks are to compensate for the CIC filter's non-flat pass band. The cascaded-filter architecture has valuable benefits. For example, with decimation, you can greatly reduce computational complexity of narrowband low pass filtering compared with if you'd used a single low pass finite impulse response (FIR) filter.

In addition, the follow-on FIR filter operates at reduced clock rates minimizing power consumption in high-speed hardware applications. A crucial bonus in using CIC filters, and a characteristic that makes them popular in hardware devices, is that they require no multiplication. The arithmetic needed to implement these digital filters is strictly additions and subtractions only.

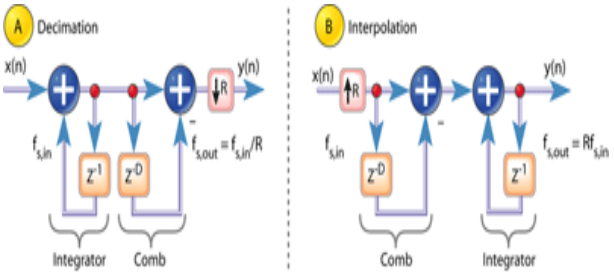

Fig.5 COMB structure for Interpolator and Decimator

If we condense the delay-line representation and ignore the 1/*D* scaling, we can obtain the classic form of a 1st-order CIC filter. The feed forward portion of the CIC filter is called the *comb* section, whose differential delay is *D*, while the feedback section is typically called an *integrator*. The comb stage subtracts a delayed input sample from the current input sample, and the integrator is simply an accumulator. The CIC filter's difference equation is: **Y (n) =x (n)-x (n-d) +y (n-1).**

In CIC filters, the comb section can precede, or follow, the integrator section. It's sensible, however, to put the comb section on the side of the filter operating at the lower sample rate to reduce the storage requirements in the delay. Swapping the comb filters from Figure 5, with the rate-change operations results in the most common implementation of CIC filters.

The decimation filter's comb section now has a delay length (differential delay) of $N = D/R$. That's because an *N*-sample delay after decimation by *R* is equivalent to a *D*-sample delay before decimation by *R*. Likewise for the interpolation filter; an *N*-sample delay before interpolation by *R* is equivalent to a *D*-sample delay after interpolation by *R*. The comb section's differential delay design parameter *N* is typically 1 or 2 for high sample-rate ratios as is often used in up/down-converters. *N* effectively sets the number of nulls in the frequency response of a decimation filter.

An important characteristic of a CIC decimator is that the shape of the filter response changes is small. For values of *R* larger than roughly 16, the change in the filter shape is

negligible. This allows the same compensation FIR filter to be used for variable-decimation ratio systems.

The CIC filter suffers from register overflow because of the unity feedback at each integrator stage. The overflow is of no consequence as long as the following two conditions are met. The range of the number system is greater than or equal to the maximum value expected at the output, and the filter is implemented with two's complement (non saturating) arithmetic.

Because a 1st-order CIC filter has a gain of $D = NR$ at 0Hz (DC), M cascaded CIC decimation filters have a net gain of $(NR)^M$. Each additional integrator must add another NR bits width for stages. Interpolating CIC filters have zeros inserted between input samples reducing its gain by a factor of $1/R$ to account for the zero-valued samples, so the net gain of an interpolating CIC filter is $(NR)^M/R$. Because the filter must use integer arithmetic, the word widths at each stage in the filter must be wide enough to accommodate the maximum signal (full-scale input times the gain) at that stage.

Although the gain of an Mth-order CIC decimation filter is $(NR)^M$, individual integrators can experience overflow. As such, the use of two's complement arithmetic resolves this overflow situation just so long as the integrator word width accommodates the maximum difference between any two successive samples. Using the two's complement binary format, with its modular wrap-around property, the follow-on comb filter will properly compute the correct difference between two successive integrator output samples.

For interpolation, the growth in word size is one bit per comb filter stage and overflow must be avoided for the integrators to accumulate properly. So, we must accommodate an extra bit of data word growth in each comb stage for interpolation. There is some small flexibility in discarding some of the least significant bits (LSBs) within the stages of a CIC filter, at the expense of added noise at the filter's output. While the preceding discussion focused on hard-wired CIC filters, these filters can also be implemented with programmable fixed-point DSP chips. Although those chips have inflexible data paths and word widths, CIC filtering can be advantageous for high sample-rate changes. Large word widths can be accommodated with multiword additions at the expense of extra instructions. Even so, for large sample-rate change factors the computational workload per output sample, in fixed-point DSP chips, may be small.

E. Compensation Filter

In typical decimation/interpolation filtering applications we want reasonably flat pass band and narrow transition-region filter performance. These desirable properties are not provided by CIC filters alone, with their drooping pass band gains and wide transition regions. We alleviate this problem, in decimation for example, by following the CIC filter with compensation non recursive FIR filter to narrow the output bandwidth and flatten the pass band gain.

The compensation FIR filter's frequency magnitude response is ideally an inverted version of the CIC filter pass band response similar to that shown by the dashed curve. If either the pass band bandwidth or CIC filter order increases the correction becomes greater, requiring more compensation FIR filter taps.

A wideband correction also means signals near $f_{s,\,out}/2$ are attenuated with the CIC filter and then must be amplified in the correction filter, adding noise. As such, practitioners often limit the pass band width of the compensation FIR filter to roughly 1/4 the frequency of the first null in the CIC-filter response.

Here's the bottom line of our CIC-filter discussion: a decimating CIC filter is merely a very efficient recursive implementation of a moving-average filter, with NR taps, whose output is decimated by R. Likewise, the interpolating CIC filter is insertion of R-1 zero samples between each input sample followed by an NR-tap moving-average filter running at the output sample rate $f_{s,\,out}$.

The cascade implementations result in total computational workloads far less than using a single FIR filter alone for high sample-rate-change decimation and interpolation. CIC filter structures are designed to maximize the amount of low-sample-rate processing to minimize power consumption in high-speed hardware applications. Their performance allows us to state that, technically speaking, CIC filters are lean, mean filtering machines.

III SIGNIFICANCE AND IMPLEMENTATION OF CONFIGURABLE SDR

The figure.6 shows the co-processing architecture for SDR. The SDR baseband processing often requires both processors and FPGAs, where the processor handles system control and configuration functions while the FPGA implements the computationally-intensive signal processing data path and control, minimizing the latency in the system. To go between standards, the processor can switch dynamically between major sections of software while the FPGA can be completely reconfigured, as necessary, to implement the data path for the particular standard.

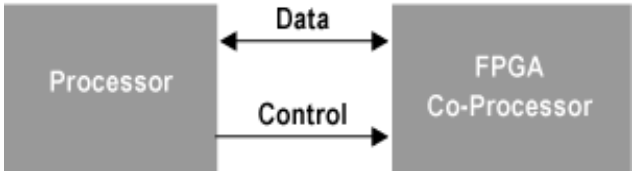

Fig.6 Co-Processing Architecture for SDR

The significance of using FPGA is that the code can be configured dynamically, thus making the hardware flexible like software. The same hardware can be used for multiple applications. It also leads to the ASIC development.

The significance of using Cascaded integrator-comb (CIC) filter, a CIC has both advantages and disadvantages compared to FIR filters. In cases where only a small amount of interpolation or decimation are needed, FIR filters generally have the advantage. However, when rates change by a factor of 10 or more, achieving a useful FIR filter anti-aliasing stop band requires exponentially increasing numbers of FIR taps.

For large rate changes, a CIC has a significant advantage over a FIR filter with respect to architectural and computational efficiency. Additionally, CIC filters can typically be reconfigured for different rates by changing nothing more than the decimation/interpolation section assuming the bit width of the integrators and comb sections meets certain mathematical criteria based on the maximum possible rate change.

IV. RESULTS AND CONCLUSIONS

The delay involved with this CIC filter is greatly reduced with other types as, it requires no multiplication. So, these digital filters achieved higher speeds of operation. The DUC performed pulse shaping and modulation of an intermediate carrier frequency at a reasonable level. The cascaded-filter architecture has brought valuable benefits. The complexity of narrow band filtering is greatly reduced using this design.

An important observation the CIC decimator is that the shape of the filter response changes in small. Particularly for the values of *R* larger than 16, the change in the filter shape is negligible. The simulation results are in well agreement with the theoretical responses of the respective outputs of different units of the SDR design, which are evident from the figures 7, 8, 9 and 10.

CIC filter structures can be designed to achieve good amount of performance at small amount of interpolation and decimation and even the better values of power consumption can be achieved in high-speed hardware applications.

ASIC solution would be a low-power and cost effective.

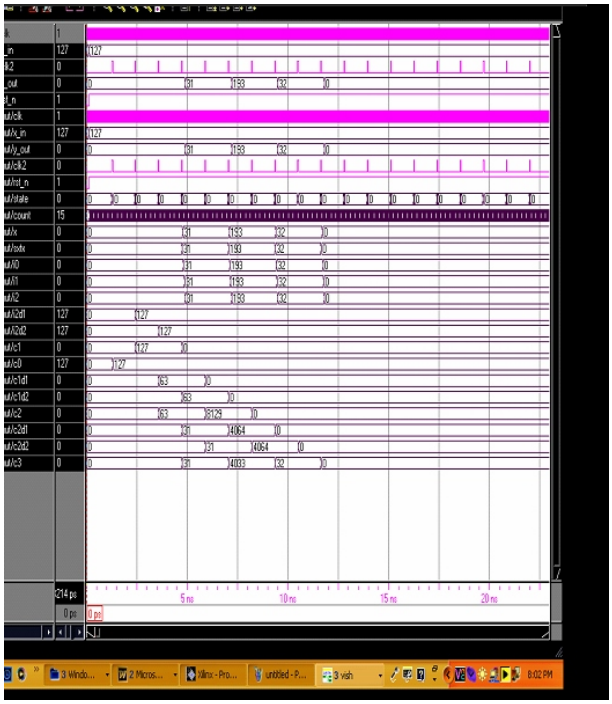

Fig .7. CIC-Decimator Response

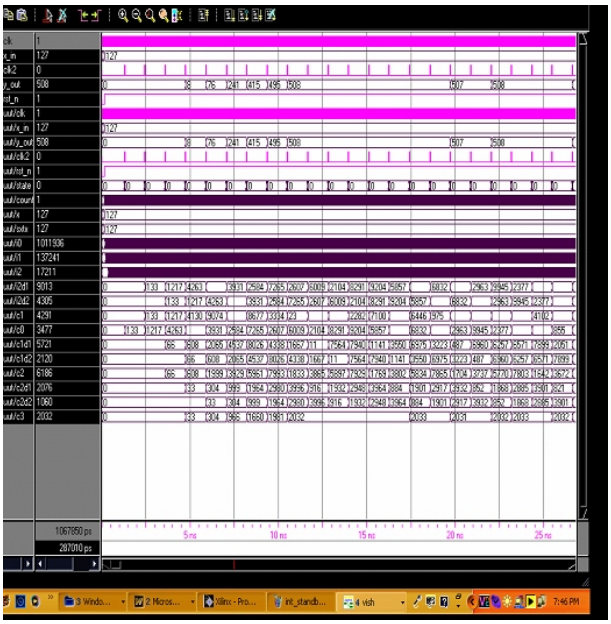

Fig. 8. CIC-interpolator output

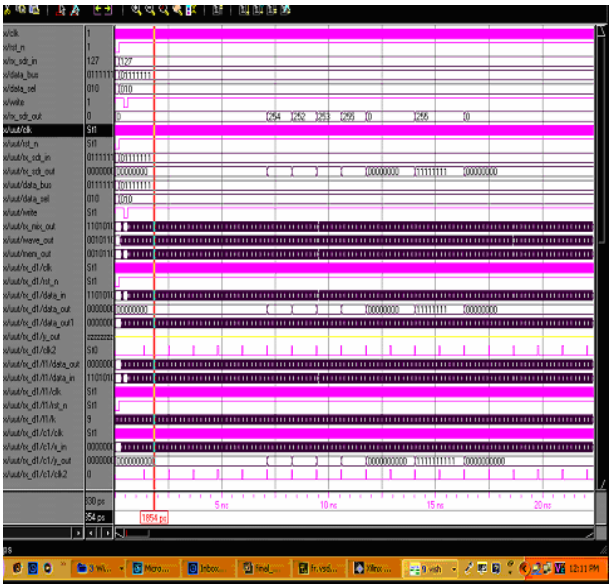

Fig. 9. Digital Down converter output

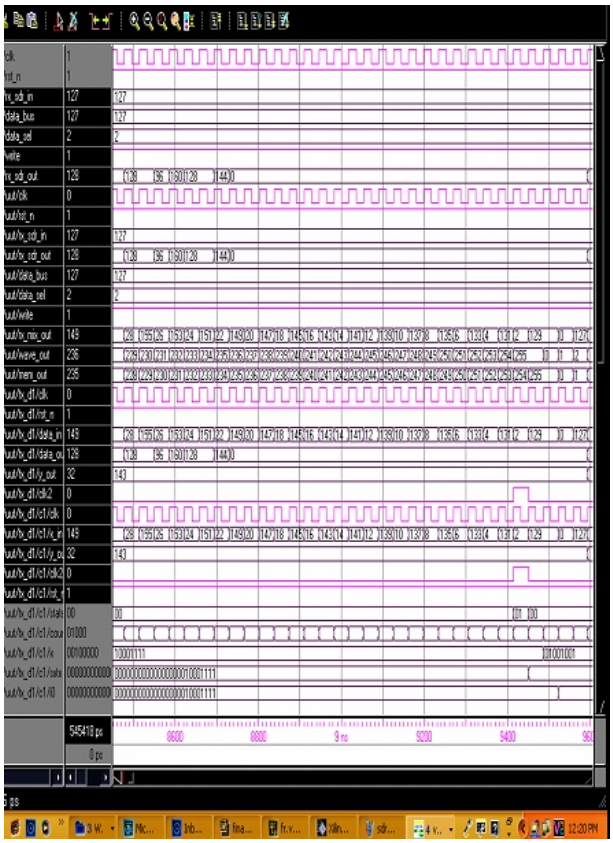

Fig .10. Digital UP converter output

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